AB8500
User manual

Mixed signal multimedia and power management

Preliminary Data

Power management module

- DB8500 modem, AP9500 application engine and multimedia processor
  - Four step down converters for processors and core with voltage scaling control
  - Two LDOs for high speed interfaces and PLLs.
  - Dynamic voltage frequency scaling
- General purpose step down
  - Two step down for I/O peripherals (1.2 V / 1.2 A, 1.8 V / 1.2 A)
- LDO for peripherals
  - Vaux1 / Vaux2: (1.1 V to 3.3 V / 200 mA)
  - Vaux3: (1.2 V to 2.91 V / 400 mA)
  - VRF1: (1.8 V to 2.5 V / 50 mA) for RF device
  - VrefDDR: Double Data Rate (DDR) reference supply
  - VAmic1, 2 for analog microphones
  - VDmic for digital microphones

Charger

- 1.5 A Constant Current/Constant Voltage (CC/CV) step down wall adapter
- 1.5 A CC/CV step down USB charger
- Coulomb counter

Audio

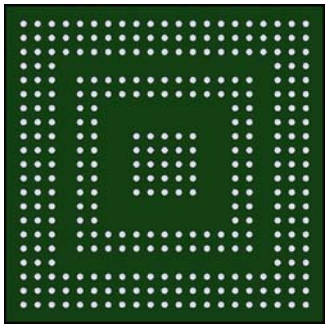
- Stereo codec with DAC SNR > 100 dB
- FIFO buffer for extended playback time
- Two TDM eight-channel interfaces (configurable in I^{2}S™ and Pulse Code Modulation (PCM))
- Two switchable differential mono microphone inputs
- Two switchable differential mono line/microphone inputs
- Stereo differential input
- Six digital microphones capability
- AB class headset capless stereo amplifier
- AB class earpiece differential amplifier
- One W D class loudspeaker stereo amplifier
- Two D class vibrator differential amplifiers

USB 2.O High Speed OTG interface

- 480 Mbit/s, 12 Mbit/s, 1.5 Mbit/s OTG transceiver (V2.0)
- UART mode
- ULPI interface
- 200 mA VBUS step up
- Supports Accessory Charger Adapter (ACA)

TVout

- Composite Video Baseband Signal (CVBS) output
- Supports all PAL and NTSC TV standards
- TV/VCR plug insertion detection



9 mm x 9 mm x 1.0 mm / 0.4 mm pitch
285 I/O - 4c - 40 G/T

SIM card interface

- 1.8 V, 3 V supply and level shifters (1.2 V optional support available)
- Supports ISO and IC-USB interfaces

General purpose analog digital converter

- Main and backup battery monitoring
- Battery and application temperature measurements
- Two accessory detection and two auxiliary inputs
- GSM burst information input

Clock management

- 32 kHz oscillator with Real-Time Clock (RTC)
- 32 kHz clock distribution
- Audio clock generation from 32 kHz in Music playback mode (in headset)
- System clock request management

Miscellaneous

- Three Pulse Width Modulation (PWM) outputs
- Temperature shutdown
- SPI or I^{2}C interface for control
- Dedicated I^{2}C buses for dynamic voltage control
- Main and Backup battery control

Applications

- DB8500 / AP9500 and multimedia processor
- 3G feature phone, smartphones

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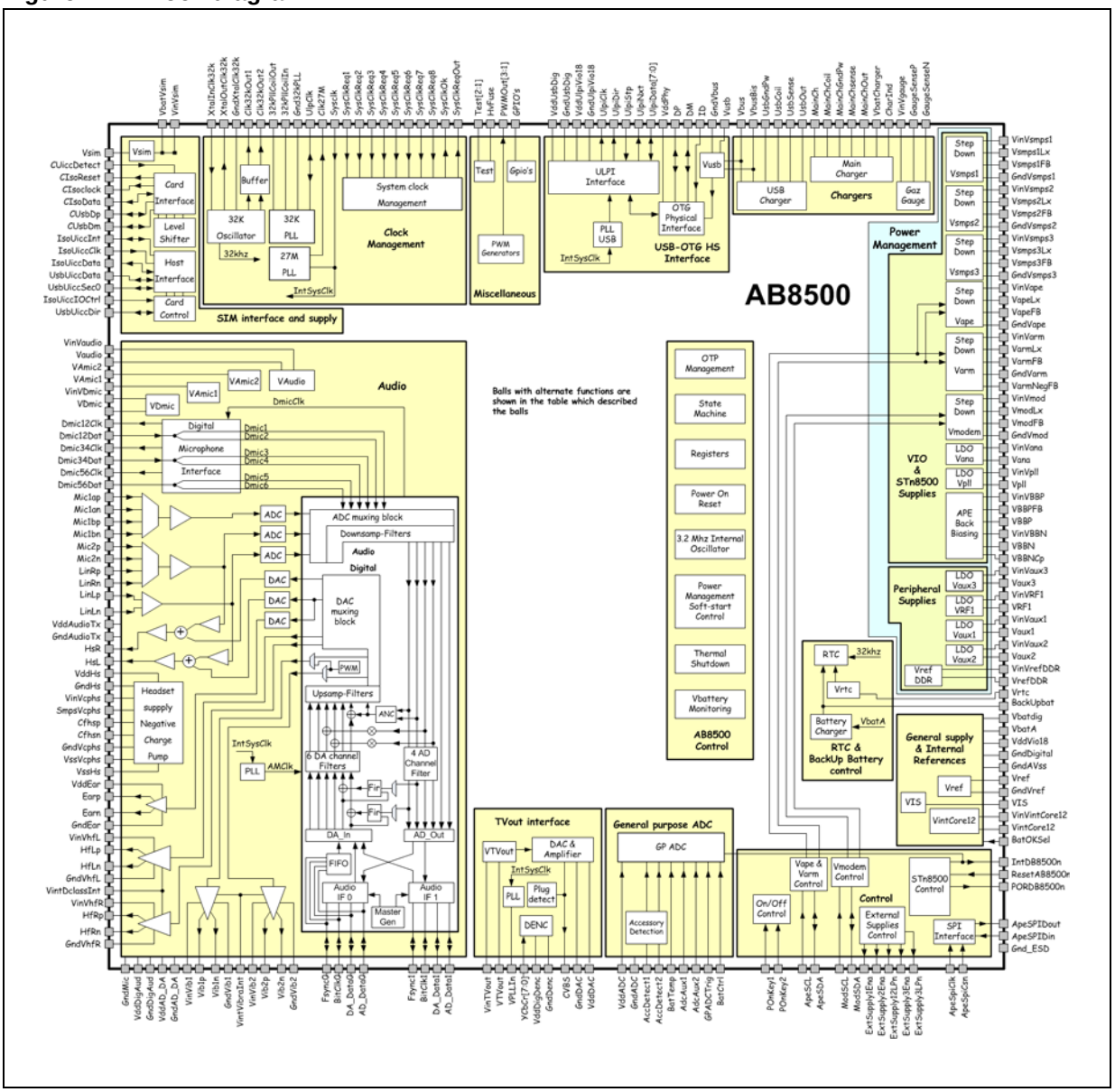
1 Block diagram

Figure 1. Block diagram



2 Ball description

Ball types:

VddD, VddA: digital, analog supply

GndD, GndA: digital, analog ground

DI, DO, DIO: digital input, output, input output

PU, PD: pull-up, pull-down

NMos I: NMOS input

OD: open drain output

AI, AO, AIO: analog input, output, input output

Table 1. Ball description

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
Control						
	General control					
C5	POnKey1	DI 100 kΩ PU	DI 100 kΩ PU	Vbat	On/Off key1	On/Off key pressure (active low)
C4	POnKey2	DI 100 kΩ PU	DI 100 kΩ PU	Vbat	Peripheral	Additional power ON/OFF control (active low)
D2	ExtSupply1Ena	DO	DO at high or low level depend of OTP settings	Vbat	Peripheral	External Vio enable if used (or other external supply)
C2	ExtSupply2Ena	DO		Vbat	Peripheral	External Vcore (or other external supply) enable if used
E5	ExtSupply3Ena	DO		Vbat	Peripheral	External Buck boost (or other external supply) enable if used
J17	ExtSupply12LPn / ExtSupply12Clk	DO		Vio18	Peripheral	Clock / Low Power command (active low) for external supply 1&2 (Vio18 and Vcore or other ext. supply)
F13	ExtSupply3LPn / ExtSupply3Clk	DO		Vio18	Peripheral	Clock / Low Power command (active low) for external supply (buck boost or ext. supply)
	DB8500 / AP9500 control					
U10	ResetAB8500n	DI	DI	Vio18	DB8500 / AP9500	AB8500 reset (active low)
U14	PORDB8500n	DO	DO High Level	Vio18	DB8500 / AP9500	DB8500 / AP9500 reset (active low)
N17	IntDB8500n	DO/OD	DO High or Low Level(1)	Vio18	DB8500 / AP9500	AB8500 Interrupt to DB8500 / AP9500 (active low)

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
A17	ApeSpiClk/ GPIO36	DI/DIO	DI	Vio18	DB8500 / AP9500	SPI clock / GPIO36
E15	ApeSpiCSn/ GPIO37	DI/DIO	DI	Vio18	DB8500 / AP9500	SPI chip select / GPIO37
C17	ApeSpiDout/ GPIO38	DO/DIO	DO HIZ	Vio18	DB8500 / AP9500	SPI data out / GPIO38
E16	ApeSpiDin/ GPIO39	DI/DIO	DI	Vio18	DB8500 / AP9500	SPI data in / GPIO39
V19	ApeSCL	DI	DI 350 Ω PU	Vio18	DB8500 / AP9500	Dedicated link - “PRCMU I2C clock” for DB8500 / AP9500 APE supplies voltage control
V20	ApeSDA	OD/DI	DI 350 Ω PU	Vio18	DB8500 / AP9500	Dedicated link “PRCMU I2C data” for DB8500 / AP9500 APE supplies voltage control
T19	ModSCL/ GPIO40	DI/DIO	DI 350 Ω PU	Vio18	DB8500 / AP9500	I2C clock for DB8500 Modem supplies voltage selection and SIM register access / GPIO40
U19	ModSDA/ GPIO41	OD, DI/DIO	DI 350 Ω PU	Vio18	DB8500 / AP9500	I2C data for DB8500 Modem supplies voltage selection and SIM register access / GPIO41
C3	BatCtrl	AI 80 kΩ PU	AI 80 kΩ PU	Vrtc	Battery	Battery control / Battery type
	Clock management					
B10	XtalInClk32K	AI			32 kHz xtal	32 kHz internal oscillator input
C10	XtalOutClk32K	AO			32 kHz xtal	32 kHz internal oscillator output
C9	GndXtalClk32K	GndA		Ground		32 kHz internal oscillator ground
J16	Clk32kOut1	DO	DO	Vio18	DB8500 / AP9500	32 kHz clock for DB8500 / AP9500
H17	Clk32kOut2	DO	DO	Vio18	Peripheral	32 kHz clock for peripheral devices
A11	32kPllCoilOut	AIO			coil	Ulp clock PLL coil connection
A10	32kPllCoilIn	AIO			coil	Ulp clock PLL coil connection
C8	Gnd32kPll	GndA		Ground		Ulp clock PLL ground
T8	SysClkReq1	DI	DI	Vio18	DB8500 / AP9500	System clock requested from DB8500 / AP9500.
T10	SysClkReq2 / GPIO1	DI/DIO	DI	Vio18	Peripheral	System clock requested from peripheral devices, or GPIO1
T9	SysClkReq3 / GPIO2	DI/DIO	DI	Vio18	Peripheral	System clock requested from peripheral devices, or GPIO2

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
U9	SysClkReq4 / GPIO3	DI/DIO	DI	Vio18	Peripheral	System clock requested from peripheral devices, or GPIO3
U2	SysClkReq5 / GPIO42	DI/DO	DI	Vio18	Peripheral	System clock requested from peripheral devices or GPIO42
W2	SysClkReq6 / GPIO4	DI/DIO	DI	Vio18	Peripheral	System clock requested from peripheral devices or APE or GPIO4
T14	SysClkReq7 / GPIO24	DI/DIO	DI	Vio18	Peripheral	System clock request or GPIO24
R16	SysClkReq8 / GPIO25	DI/DIO	DI	Vio18	Peripheral	System clock request or GPIO25
V3	SysClkOk	DO	DO High Level	Vio18	DB8500 / AP9500	System clock O.K signal to DB8500 / AP9500
Y2	SysClkReqOut	DO	DO High Level	Vio18	RF	External RF clock generators enable
U17	HiqClkEna/ GPIO10	DO/DIO	DI 50 kΩ PD	Vio18	RF	External high quality clock enable or GPIO10
L16	SysClk	DI	DI	Vio18	RF	System clock input square
F21	UlpClk	DIO	DI 50 kΩ PD	Vio18	DB8500 / AP9500	Ultra Low Power system clock output to DB8500 / AP9500
T16	Clk27M	DIO	DI 50 kΩ PD	Vio18	DB8500 / AP9500	27 MHz video clock to DB8500 / AP9500
Power management						
	AB8500 internal supplies					
E8	VbatDig	VddA		Vbat	Capacitor	
D1 W14	VbatA_1 VbatA_2	VddA		Vbat	Capacitor	
R19	BattOkSel	DI	DI	Vbat		BattOk comparator threshold selection (for 2.3 V / 2.7 V battery types)
U6 K16	VddVio18_1 VddVio18_2	VddD		Vio18	Ext. Switched-Mode Power Supply (SMPS) or Vio18	1.8 V IO internal supply
K13	GndDigital	GndD		ground		Digital grounds

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
J10 J11 J12 K9 K11 K12 L9 L11 L12 M10 M11 M12 M13 N9 N10 N12 U20	GndAvss	GndA		ground		Analog grounds
J9 K10 N11	Gnd_ESD	GndA		ground		ESD ring grounds
F9	Vrtc	AO			Capacitor	32 kHz internal oscillator and RTC supply
W12	GndVref	GndA		ground		1.8 V internal reference ground
E7	Vref	AO			Capacitor	1.8 V internal reference
B16	VIS	AO			Capacitor	Internal Supply
A8	VinVintCore12	VddA		Vbat	Capacitor	Vint input power supply
B8	VintCore12	AO			Capacitor	LDO output dedicated to supply AB8500 USB digital part
	DB8500 / AP9500 and I/O's supplies					
Y17 AA17	VinVape	VddA		Vbat	Capacitor	Vape input power supply balls
Y16 AA16	VapeLx	AO			Coil	Vape external coil connection balls
W16	VapeFB	AI	Default output value		Capacitor	Vape feedback and DB8500 / AP9500 supply
Y15 AA15	GndVape	GndA		ground	Power ground	Vape ground balls
N20 N21	VinVarm	VddA		Vbat	Capacitor	Varm input power supply balls
P20 P21	VarmLx	AO			Coil	Varm external coil connection balls

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
T21	VarmFB	AI	Default output value		Capacitor	Varm feedback and DB8500 / AP9500 supply
N19 P19	GndVarm	GndA		ground	Power ground	Varm ground balls
T20	VarmNegFB	AI				Varm negative voltage feedback
Y11 AA11	VinVmod	VddA		Vbat	Capacitor	Vmod input power supply balls
Y10 AA10	VmodLx	AO			Coil	Vmod external coil connection balls
Y12	VmodFB	AI	Default output value		Capacitor	Vmod feedback and DB8500 / AP9500 supply
Y9 AA9	GndVmod	GndA		ground	Power ground	Vmod ground balls
B1 C1	VinVsmps1	VddA		Vbat	Capacitor	Vsmps1 input power supply balls
A2 A3	Vsmps1Lx	AO			Coil	Vsmps1 external coil connection balls
B2	Vsmps1FB	AI			Capacitor	Vsmps1 feedback and Vio12 supply
A4 B4	GndVsmps1	GndA		ground	Power ground	Vsmps1 ground balls
U1 V1	VinVsmps2	VddA		Vbat	Capacitor	Vsmps2 input power supply balls
R1 T1	Vsmps2Lx	AO			Coil	Vsmps2 external coil connection balls
V2	Vsmps2FB	AI			Capacitor	Vsmps2 feedback and Vio18 supply
R2 T2	GndVsmps2	GndA		ground	Power ground	Vsmps2 ground balls
A5 B5	VinVsmps3	VddA		Vbat	Capacitor	Vsmps3 input power supply ball
A6 B6	Vsmps3Lx	AO			Coil	Vsmps3 external coil connection ball
C6	Vsmps3FB	AI	Default output value		Capacitor	Vsmps3 feedback and DB8500 / AP9500 Vsafe supply
A7 B7	GndVsmps3	GndA		ground	Power ground	Vsmps3 ground ball
E1	VinVana	VddA		Vbat	Capacitor	Vana input power supply

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
D3	Vana	AO			Capacitor	Vana LDO output and DB8500 / AP9500 supply
A9	VinVpll	VddA		Vbat	Capacitor	Vpll input power supply
B9	Vpll	AO			Capacitor	Vpll LDO output for internal clock tree and DB8500 / AP9500 PLL
Y19	VinVBBP	VddA		Vbat	Capacitor	VBBP input power supply
U15	VBBP	AO	Varm		Capacitor	VBBP LDO output for DB8500 / AP9500 P-Type devices reverse/forward bias
U21	VBBPFB	AI		Varm	Capacitor	Varm voltage feedback
T15	VBBN	AO	GndA		Capacitor	VBBN LDO output for DB8500 / AP9500 N-Type devices reverse/forward bias
W19	VBBNCp	AO			Capacitor	VBBNCp charge pump output
Y20	VinVBBN	VddA		Vio18	Capacitor	VBBN input power supply
	Peripheral supplies					
Y21	VinVrefDDR	AO		Vsmps1	Capacitor	VrefDDR input supply
W21	VrefDDR	AO			Capacitor	VrefDDR supply
C11	BackUpBat	AIO			Backup battery	Backup battery supply
E9	VinVRF1	VddA		Vbat	Capacitor	VRF1 input power supply
B11	VRF1	AO	Default output value		Capacitor	VRF1 LDO output for system clock oscillator
AA12	VinVaux1	VddA		Vbat	Capacitor	Vaux1 input power supply
AA13	Vaux1	AO	Software dependent		Capacitor	Vaux1 LDO output for peripheral devices
AA14	VinVaux2	VddA		Vbat	Capacitor	Vaux2 input power supply
Y13	Vaux2	AO	Software dependent		Capacitor	Vaux2 LDO output for peripheral devices
W11	VinVaux3	VddA		Vbat	Capacitor	Vaux3 input power supply
W13	Vaux3	AO	Software dependent		Capacitor	Vaux3 LDO output for peripheral devices
Energy management						
	Wall charger					
G21 H20 H21 J20	MainCh	VddA			Capacitor	Main charger cable

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
J21 K20 K21	MainChCoil	AIO			Coil	Main charger external coil connection balls
L20 L21 M21	MainChGndPw	GndA		ground	Power ground	Main charger power ground
M19	VbatCharger	VddA		Vbat		Charger feature input supply
C16	CharInd	AO			Ext. LED	Charging indication
K19	MainChSense	AI			Resistor	Main charger sense resistor (coil connection)
L19	MainChOut	AI			Resistor	Main charger sense resistor (battery connection)
	USB charger					
A13 B13 C13	Vbus	AO			Capacitor	USB cable
A14 A15 B14	UsbCoil	AIO			Coil	USB external coil connection balls
B15 C14 C15	UsbGndPw	Gnd		ground	Power ground	USB charger power ground
C19	UsbSense	AI			Resistor	USB sense resistor (coil connection)
B18	UsbOut	AI			Resistor	USB sense resistor (battery connection)
A16	VbusBis	AO			Capacitor	Vusb LDO supply
	Coulomb counter					
U13	VinGauge	VddA		Vbat	Capacitor	
U12	GaugeSenseP	AI			Resistor	Gauge sense positive input
T13	GaugeSenseN	AI		ground	Resistor	Gauge sense negative input
AB8500 multimedia features						
	Audio					
F1	VinVaudio	VddA		Vbat	Capacitor	Vaudio input power supply
G1	Vaudio	AO			Capacitor	Vaudio LDO output dedicated to internal analog audio
F3	VddAudioTx	AI		Vaudio		Audio transmit paths positive supply
E2	GndAudioTx	GndA		ground		Audio transmit paths ground

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
T3	VddDigAud	AI		Vio12	Capacitor	Digital positive supply (1.2 V nominal) connected at PCB level at Vio12 output
U3	GndDigAud	GndD		ground		Audio digital ground (Thermal Ball)
L1	VddAD_DA	AI		Vaudio		Positive supply for all analog blocks except output drivers, must be connected to Vaudio ball
K2	GndAD_DA	GndA		ground		Ground for all analog blocks except output drivers
M1	VddEar	AI		Vbat or Vaudio or external supply	Capacitor	Positive Supply for Earphone, EAR class AB output driver. It must be externally connected to Vaudio supply voltage ball.
M5	GndEar	GndA		ground		Ground for Earphone, EAR class AB output driver
M9	GndMic	GndA		ground		Ground for analog microphone amplifier
N1	VddHs	AI		Vaudio or Vio18		Positive supply for stereo headset (HS) class AB output driver. It must be externally connected to Vaudio supply voltage ball
L2	GndHs	GndA		ground		Ground for stereo HS class AB output drivers. This ball is used as headset voltage reference.
P1	VinVcphs	VddA		Vbat	Capacitor	Positive supply for charge pump circuit. It can be connected directly to the battery.
R3	SmpsVcphs	VddA		Vio18	Capacitor	Positive supply for charge pump circuit. It can be connected to Vsmps2.
N3	Cfhsp	AIO			Capacitor	Charge pump external capacitor positive pin
P3	Cfhsn	AIO			Capacitor	Charge pump external capacitor negative pin. Negative voltage tolerant ball.
P2	GndVcphs	GndA		ground		Ground for charge pump circuit.
M6	VssVcphs	AO		VssA	Capacitor	Negative supply output for headset drivers.
G3	VinVDmic	VddA		Vbat	Capacitor	Vdmic input supply

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
M3	VssHs	AI		VssA	VssVcphs	Negative supply for stereo HS class AB output drivers. It must be externally connected to VssVcphs negative supply ball
G2	VAmic1	AO			Capacitor	Low noise reference output voltage for analog microphone biasing
K1	VAmic2	AO			Capacitor	Low noise reference output voltage for analog microphone biasing
F2	VDmic	AO			Capacitor	Supply voltage output for up to six digital microphones
Y7	VinDclassInt	VddA		Vbat	Capacitor	Supply for class D amplifiers. Can be connected directly to the most positive supply. (Battery) Note: VinDclassInt, VinVhfl, VinVhfr must be connected to the same supply voltage.
Y8	VinVhfR	VddA		Vbat	Capacitor	Positive supply for Handsfree Right (HFR) class D output driver. Can be connected directly to the battery
Y6	VinVhfL	VddA		Vbat	Capacitor	Positive supply for Handsfree Left (HFL) class D output driver. Can be connected directly to the battery
Y4	VinVibraInt	VddA		Vbat	Capacitor	Supply for class D amplifiers. Can be connected directly to the most positive supply. (Battery) Note: VinVibraInt, VinVib1, VinVib2 must be connected to the same supply voltage.
AA2	VinVib1	VddA		Vbat	Capacitor	Positive supply for VIB1 class D output driver. Can be connected directly to the battery
W4	VinVib2	VddA		Vbat	Capacitor	Positive supply for VIB2 class D output driver. Can be connected directly to the battery
U8	GndVhfR	GndA		ground		Ground for Hands-Free HFR class D output driver
W7	GndVhfL	GndA		ground		Ground for Hands-Free HFL class D output driver
W3	GndVib1	GndA		ground		Ground for VIB1 class D output driver
Y5	GndVib2	GndA		ground		Ground for VIB2 class D output driver

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
J5 H5 J3 H3	LinLp LinLn LinRp LinRn	AI				Stereo differential line input balls
H1 J1	Mic1ap Mic1an	AI				Mono differential microphone input balls
J2 H2	Mic1bp Mic1bn	AI				Mono differential microphone input balls
L3 K3	Mic2p Mic2n	AI				Mono differential microphone input balls
J6 K6	Dmic12Clk/ GPIO27 Dmic12Dat/ GPIO28	DO/DIO DI/DIO	DO 50k PD DI 50k PD	VDmic		Master clock output for digital microphones 1 and 2 or GPIO27 Multiplexed stereo input for digital microphones 1 and 2 or GPIO28
G6 H6	Dmic34Clk/ GPIO29 Dmic34Dat/ GPIO30	DO/DIO DI/DIO	DO 50k PD DI 50k PD	VDmic		Master clock output for digital microphones 3 and 4 or GPIO29 Multiplexed stereo input for digital microphones 3 and 4 or GPIO30
F5 G5	Dmic56Clk/ GPIO31 Dmic56Dat/ GPIO32	DO/DIO DI/DIO	DO 50k PD DI 50k PD	VDmic		Master clock output for digital microphones 5 and 6 or GPIO31 Multiplexed stereo input for digital microphones 5 and 6 or GPIO32
AA7 AA6 W9 AA8	HfLp HfLn HfRp HfRn	AO				Differential stereo Class D outputs for Handsfree Speakers
L5 K5	Earp Earn	AO				Differential mono Class AB output for earphone speaker
M2 N2	HsL HsR	AO				Single-ended stereo ground-centered Class AB outputs for headset speakers
AA4 AA3	Vib1p Vib1n	AO				Differential mono Class D output for Melody/Vibra1 functions
W5 AA5	Vib2p Vib2n	AO				Differential mono Class D output for Melody/Vibra2 functions
T6 R6 P6 N6	Fsync0 BitClk0 DA_Data0 AD_Data0/ IntAudn	DIO	DI	Vio18	DB8500	Audio data Interface 0 (Note: AD_Data ball configured as interrupt, IntAudn, when internal audio FIFO is used)

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
P5 R5 U5 T5	AD_Data1/ GPIO17 DA_Data1/ GPIO18 Fsync1/GPIO19 BitClk1/GPIO20	DIO	DI	Vio18	Peripheral	Audio data Interface 1 or GPIO17 to GPIO20
	USB OTG transceiver					
E13	Vusb	AO			Capacitor	Vusb LDO output dedicated to internal USB physical layer
F16	VddPHY	VddA		Vusb		USB PHY supply
E14	VddUsbDig	VddD		Vint Core12	Capacitor	Digital positive supply (1.2 V nominal) connected to VintCore12 ball
J13	GndUsbDig	GndD		ground		USB digital ground
J19	VddUlpiVio18	VddD		Vio18	Capacitor	ULPI IOs digital supply
E17	GndUlpiVio18	GndD		ground		ULPI interface ground
C18	GndVbus	GndA		ground	USB connector	Analog USB interface ground
A20	DP	AIO		Vusb	USB connector	USB positive data
A19	DM	AIO		Vusb	USB connector	USB negative data
B19	ID	AI		Vusb	USB connector	USB ID
D19	UlpiClk	DO	DO	Vio18	DB8500 / AP9500	ULPI Clock
F19	UlpiDir	DO	DO	Vio18	DB8500 / AP9500	ULPI direction
E19	UlpiStp	DI 100 kΩ PU	DI 100 kΩ PU	Vio18	DB8500 / AP9500	ULPI stop
B21	UlpiNxt	DO	DO	Vio18	DB8500 / AP9500	ULPI next
B20 C21 C20 D20 D21 E20 E21 F20	UlpiData[7] UlpiData[6] UlpiData[5] UlpiData[4] UlpiData[3] UlpiData[2] UlpiData[1] UlpiData[0]	DIO	DI 50 kΩ PD	Vio18	DB8500 / AP9500	ULPI data
R17	GPIO34 ExtCPEna	DIO	DI 50 kΩ PD	Vbat	Peripheral	GPIO34 or External charge pump enable
	General purpose ADC, Accessory detection					
R20	VddADC	AI		Vtvout		General purpose ADC supply

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
N13	GndADC	GndA		ground		Internal ADC ground
N16	BatTemp	AI		Vbat	Battery	Battery temperature
T12	AdcAux1	AI				ADC Auxiliary input
T11	AdcAux2	AI				ADC Auxiliary input
P16	AccDetect1	AI				ADC and Accessory detection 1 input
P17	AccDetect2	AI				ADC and Accessory detection 2 input
N5	GPADCTrig	DI 50 kΩ PD	DI 50 kΩ PD	Vio18		ADC trigger input
	TVout interface					
L17	VinVTVout	VddA		Vbat	Capacitor	VTVout input power supply
M17	VTVout	AO			Capacitor	VTVout LDO output dedicated to internal TVout.
V21	VPLLIn	AI		Vpll		TVout PLL supply
R21	VddDAC	AI		VTVout		CVBS DAC supply
L10	GndDAC	GndA		ground		CVBS DAC ground
K17	VddDigDenc	AI		Vio12	Capacitor	Digital Positive supply (1.2 V nominal) connected at PCB level at Vio12 output
L13	GndDenc	GndD		ground		DENC digital ground
W20	CVBS	AO			Resistor	Video Composite signal output
AA19 W18 AA20 Y18	YCbCr3/ GPIO9 YCbCr2 / GPIO8 YCbCr1 / GPIO7 YCbCr0 / GPIO6	DI/DIO	DI	Vio18	DB8500	Time multiplexed 4:2:2 luminance and chrominance data with synchro embedded (Dual data rate data transfer)
	SIM interface					
B12	VinVsim	VddA		Vbat	Capacitor	Vsim input power supply
A12	VbatVsim	VddA		Vbat	Capacitor	Vsim input power supply
C12	Vsim	AO			Capacitor	Vsim LDO output dedicated to SIM card supply
F10	CUiccDetect	AI		Vsim	SIM card	SIM card detection (active low)
E10	CIsoReset	DO	DO WeakPD	Vsim	SIM card	SIM card reset ball
F11	CIsoClock	DO	DO WeakPD	Vsim	SIM card	SIM card clock ball

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
E12	CIsoData	DIO	DO WeakPD	Vsim	SIM card	SIM card data
F12	CUsbDp	DIO	DI 90 kΩ PD	Vsim	SIM card	SIM card DP ball
E11	CUsbDm	DIO	DI 90 kΩ PD	Vsim	SIM card	SIM card DN ball
AA18	UsbUiccPd / GPIO11	DI/DIO	DI 50 kΩ PD	Vio18	DB8500	USBUICC Pull-down control or GPIO11
G16	IsoUiccIOCtrl	DI 50 kΩ PD	DI 50 kΩ PD	Vio18	DB8500	ISO-UICC IO direction control Low: DB8500 to SIM card High: SIM card to DB8500
F17	IsoUiccClk	DI 50 kΩ PD	DI 50 kΩ PD	Vio18	DB8500	ISO-UICC clock
H16	IsoUiccData	DIO	DI 50 kΩ PD	Vio18	DB8500	ISO-UICC data
G17	IsoUiccInt	DIO	DO Low Level	Vio18	DB8500	ISO-UICC output interrupt or reset
H19	UsbUiccDir/ Gpio21	DI/DIO	DI	Vio18	DB8500	USB-UICC IO direction control / Gpio21 Low: DB8500 to SIM card High: SIM card to DB8500
G20	UsbUiccData/ Gpio22	DIO	DI	Vio18	DB8500	USB-UICC data or DP / Gpio22
G19	UsbUiccSe0/ Gpio23	DIO	DI	Vio18	DB8500	USB-UICC SE0 or DN / Gpio23
Miscellaneous and test						
	Miscellaneous					
U16	GPIO12	DIO	DI 50k PD	Vio18	Peripheral	GPIO12
W17	GPIO13	DIO	DI 50k PD	Vio18	Peripheral	GPIO13
M16	GPIO26	DIO	DI 50k PD	Vio18	Peripheral	General purpose IO
W15	GPIO35	DIO	DI 50k PD	Vio18	Peripheral	GPIO35
F15 B17 F14	PWMOut3/ GPIO[16] PWMOut2/ GPIO[15] PWMOut1/ GPIO[14]	DO/DIO	DO	Vio18	Peripheral	PWM outputs / GPIOs

Table 1. Ball description (continued)

Ball #	Name	Dir. and conf.	State after reset	Level	From/To	Comments
	Test					
T17	Test1					Must be connected to ground
F8	Test2					Must be connected to ground
U11	HVFuse					Must be left opened i
A1 A18 A21 B3 C7 E3 E6 F6 F7 L6 M20 T7 U7 W1 W6 W8 W10 Y1 Y3 Y14 AA1 AA21	N.C.					Not connected

1. Interrupts not masked

Table 2. Ballout layout - Columns 1 to 10

	1	2	3	4	5	6	7	8	9	10
A	N.C.	Vsmps1Lx	Vsmps1Lx	Gnd Vsmps1	VinVsmps3	Vsmps3Lx	Gnd Vsmps3	VinVint Core12	VinVpll	32kPll CoilIn
B	VinVsmps1	Vsmps1FB	N.C.	Gnd Vsmps1	VinVsmps3	Vsmps3Lx	Gnd Vsmps3	VintCore12	Vpll	XtalIn Clk32k
C	VinVsmps1	ExtSupply2 Ena	BatCtrl	PonKey2	PonKey1	Vsmps3FB	N.C.	Gnd32kPll	GndXtal Clk32k	XtalOut Clk32k
D	VbatA_1	ExtSupply1 Ena	Vana							
E	VinVana	GndAudio Tx	N.C.		ExtSupply3 Ena	N.C.	Vref	VbatDig	VinVRF1	CIsoReset
F	VinVaudio	VDmic	VddAudioTx		Dmic56Clk	N.C.	N.C.	Test2	Vrtc	CUicc Detect
G	Vaudio	VAmic1	VinVDmic		Dmic56Dat	Dmic34Clk				
H	Mic1ap	Mic1bn	LinRn		LinLn	Dmic34Dat				
J	Mic1an	Mic1bp	LinRp		LinLp	Dmic12Clk			GndEsd	GndAVss
K	VAmic2	GndAD_DA	Mic2n		Earn	Dmic12Dat			GndAVss	GndEsd
L	VddAD_DA	GndHs	Mic2p		Earp	N.C.			GndAVss	GndDAC
M	VddEar	HsL	VssHs		GndEar	VssVcphs			GndMic	GndAVss
N	VddHs	HsR	Cfhsp		GPADCTrig	AD_Data0			GndAVss	GndAVss
P	VinVcphs	GndVcphs	Cfhsn		AD_Data1	DA_Data0				
R	Vsmps2Lx	Gnd Vsmps2	SmpsVcphs		DA_Data1	BitClk0				
T	Vsmps2Lx	Gnd Vsmps2	VddDigAud		BitClk1	Fsync0	N.C.	SysClk Req1	SysClk Req3	SysClk Req2
U	VinVsmps2	SysClk Req5	GndDigAud		Fsync1	VddVio18_1	N.C.	GndVhfR	SysClk Req4	Reset AB8500n
V	VinVsmps2	Vsmps2FB	SysClkOk							
W	N.C.	SysClk Req6	GndVib1	VinVib2	Vib2p	N.C.	GndVhfL	N.C.	HfRp	N.C.
Y	N.C.	SysClk ReqOut	N.C.	VinVibraInt	GndVib2	VinVhfL	VinDclass Int	VinVhfR	GndVmod	VmodLx
AA	N.C.	VinVib1	Vib1n	Vib1p	Vib2n	HfLn	HfLp	HfRn	GndVmod	VmodLx

Note: Center balls: It is recommended to connect all center ball from J9 up to N13 Ground, see layout guide lines application note for connection to Gnd (CD00252716_TN0146_RSTEP_board_layout_design_guidelines).

Table 3. Ballout layout - Column 11 to 21

	11	12	13	14	15	16	17	18	19	20	21
A	32kPll CoilOut	VbatVsim	Vbus	UsbCoil	UsbCoil	VbusBis	ApeSpiClk	N.C.	DM	DP	N.C.
B	VRF1	VinVsim	Vbus	UsbCoil	UsbGnd Pw	VIS	PWMOut2	UsbOut	ID	UlpiData7	UlpiNxt
C	BackUp Bat	Vsim	Vbus	UsbGnd Pw	UsbGnd Pw	CharInd	ApeSpi Dout	GndVbus	UsbSense	UlpiData5	UlpiData6
D									UlpiClk	UlpiData4	UlpiData3
E	CUsbDm	CIsoData	Vusb	VddUsb Dig	ApeSpi CSn	ApeSpiDin	GndUlpi Vio18		UlpiStp	UlpiData2	UlpiData1
F	CIsoClock	CUsbDp	Ext Supply3 Clk	PWMOut1	PWMOut3	VddPhy	IsoUicc Clk		UlpiDir	UlpiData0	UlpClk
G						IsoUicc Ctrl	IsoUicc Int		UsbUicc SE0	UsbUicc Data	MainCh
H						IsoUicc Data	Clk32k Out2		UsbUicc Dir	MainCh	MainCh
J	GndAVss	GndAVss	GndUsb Dig			Clk32k Out1	Ext Supply12 Clk		VddUlpi Vio18	MainCh	MainCh Coil
K	GndAVss	GndAVss	GndDigital			VddVio 18_2	VddDig Denc		MainCh Sense	MainCh Coil	MainCh Coil
L	GndAVss	GndAVss	GndDenc			SysClk	VinTVout		MainCh Out	MainCh GndPw	MainCh GndPw
M	GndAVss	GndAVss	GndAVss			GPIO26	VTVout		Vbat Charger	N.C.	MainCh GndPw
N	GndEsd	GndAVss	GndADC			BatTemp	Int DB8500n		GndVarm	VinVarm	VinVarm
P						Acc Detect1	Acc Detect2		GndVarm	VarmLx	VarmLx
R						SysClk Req8	GPIO34 ExtCPEna		BatOkSel	VddADC	VddDAC
T	AdcAux2	AdcAux1	Gauge SenseN	SysClk Req7	VBBN	Clk27M	Test1		ModSCL	Varm NegFB	VarmFB
U	HVFuse	Gauge SenseP	VinVgauge	POR DB8500n	VBBP	Gpio12	HiqClkEna		ModSDA	GndAVss	VBBPFB
V									ApeSCL	ApeSDA	VPLLIn
W	VinVaux3	GndVref	Vaux3	VbatA_2	GPIO35	VapeFB	Gpio13	YCbCr2	VBBNCp	CVBS	VrefDDR
Y	VinVmod	VmodFB	Vaux2	N.C.	GndVape	VapeLx	VinVape	YCbCr0	VinVBBP	VinVBBN	VinVref DDR
AA	VinVmod	VinVaux1	Vaux1	VinVaux2	GndVape	VapeLx	VinVape	UsbUicc Pd	YCbCr3	YCbCr1	N.C.

Note: Center balls: It is recommended to connect all from J9 up to N13 to Ground, see layout guide lines application note for connection to Gnd (CD00252716_TN0146_RSTEP_board_layout_design_guidelines).

3 Functional description

3.1 Introduction

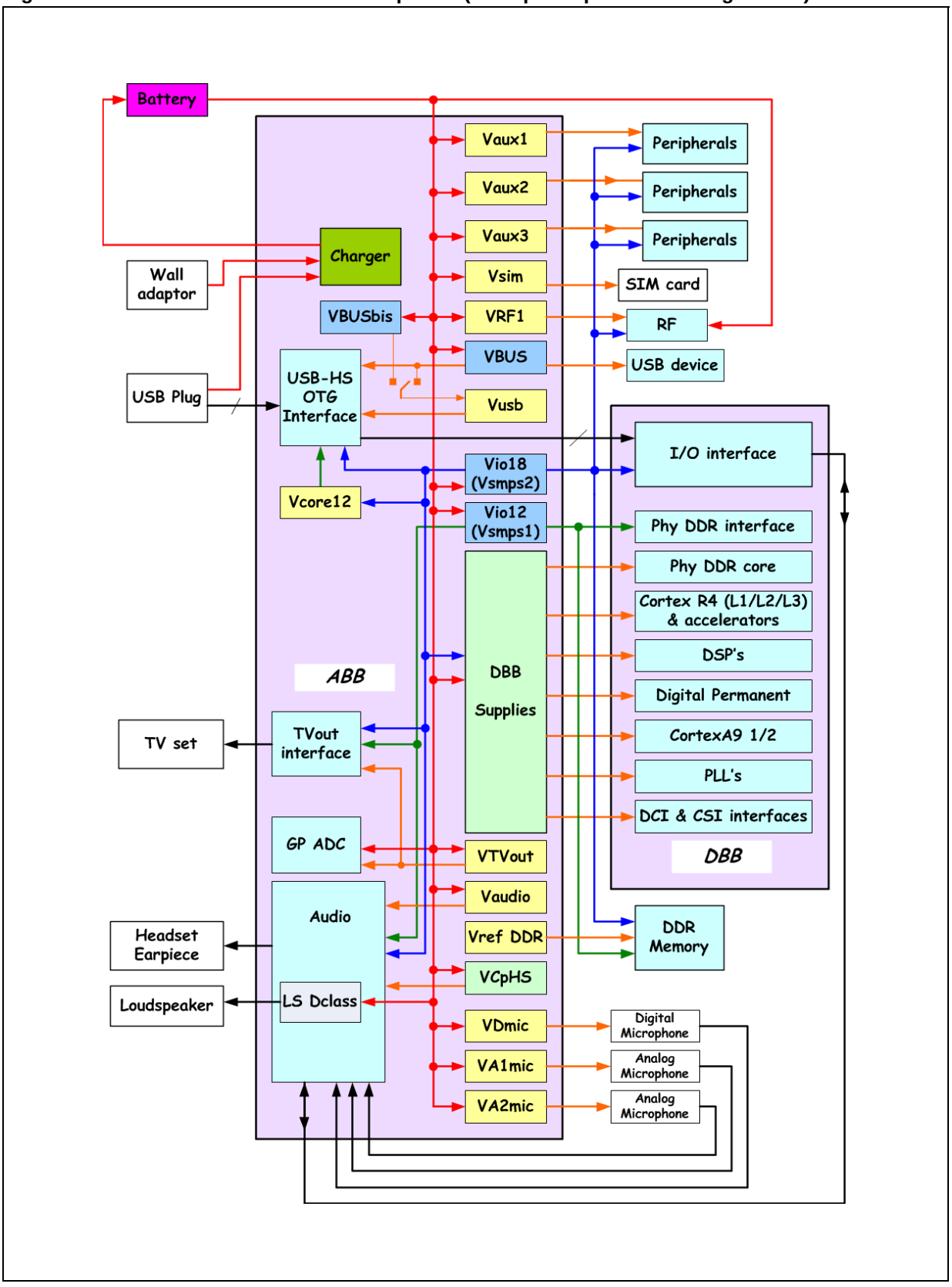
AB8500 and DB8500 / AP9500 are a set of devices dedicated to high feature phones, AP9500 is a powerful multimedia audio and video processor. In addition to AP9500, the DB8500 includes a HSPA+ modem.

AB8500 embeds the following:

- A control interface
  - ON/OFF management
  - External supply control
  - Digital interface with DB8500 / AP9500
- A clock management system
  - System clock request
  - 32 kHz oscillator / RTC
  - 38.4 MHz clock issued from 32 kHz for uses which do not request 38.4 MHz RF system clock.
- A power management module
  - DB8500 / AP9500 supplies
  - Peripheral supplies
- A charger
  - Wall charger
  - USB charger
  - Coulomb counter
  - Backup battery management
- An audio module
- A TVout module
- A USB 2.0 High Speed OTG interface
- A general purpose ADC for:
  - Accessory detection
  - Battery monitoring
  - Temperature monitoring

Figure 2 gives an example of AB8500 in a feature phone.

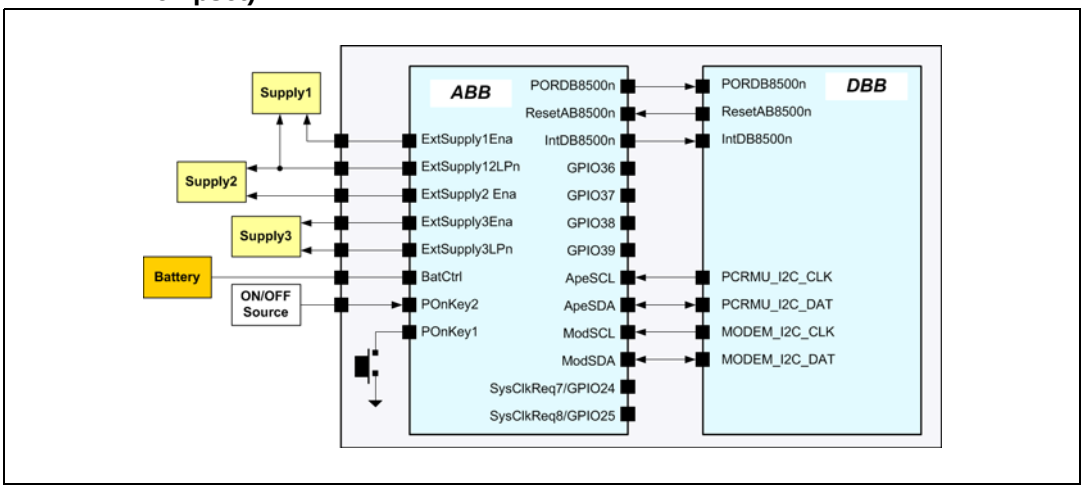
Figure 2. AB8500/DB8500 in a feature phone (example of possible configuration)



3.2 Control interface

Figure 3 describes the control interfaces.

Figure 3. Control interface AB8500/DB8500/AP9500 and AB8500/external to chipset)



3.2.1 ON/OFF management

AB8500 embeds the following:

- The ON mode control for the whole system:
  - Events to put ON AB8500, when previously in OFF mode are as follows:
    - *** POnKey1** is dedicated to ON/OFF key (‘PonKey1dbF’ bit)
    - *** POnKey2** can be used to put ON AB8500. (‘PonKey2dbF’ bit)

Note: Except for the 10-s key press behavior described below, PonKey1 and PonKey2 balls behave similarly. If, instead of a key, a digital signal is connected to PonKey2 ball, AB8500 goes to ON mode on a high/low transition signal, then the AB8500 goes to OFF mode if one of the “OFF” conditions described below is true.

  - * RTC alarm value reached. (‘RTCAlarm’ bit)
  - * Main charger plugs. (‘MainChDet’ bit)
  - * USB charger plugs. (‘VbusDet’ bit)
  - * USB ID detection. (‘UsbIDDetect’ bit)
  - Events to start AB8500, when previously in Unconfigured mode are:
    - * Battery is inserted. (‘PornVbat’ bit)
    - * Main or USB charger plug, with dead battery.

*Note: Main and USB chargers turn On events are gated by **BatCtrl** ball signal (does not occur if **BatCtrl** input is higher than 1.65 V).*

Turn On event is stored in TurnOnstatus register.

- In the OFF mode control for the whole system, events to switch OFF AB8500 are:

  Turn Off event is stored in *SwitchOffStatus* register (‘bitname’ below).

  – ON/OFF key press duration (**PonKey1** ball) is longer than 10 s timer (‘PonKey1LongF’ bit).
  – ‘SWOFF’ and ‘SwReset4500n’ bits of STw4500Ctrl1 register are simultaneously set high (‘SwOffCmd’ bit).
  – ‘The DB8500SWOff’ bit of STw4500Ctrl1 register is set high, switch off due to DB8500 / AP9500 thermal information (‘ThDB8500SwOffCmd’ bit).
  – Internal watchdog timer expires, its value is programmed between 1 and 128 s in MainWDogTimer register and its default value is 32 s (‘WdogErr’ bit).
  – Battery goes below BattOKF threshold; this threshold is programmable by OTP. If charger is still present, AB8500 is turned ON again as soon as battery rises above BattOK threshold (‘BattOkProt’ bit),
  – Thermal shutdown protection occurs (‘ThSDProt’ bit).
  – Battery removal (‘PornVbat’ bit).
  – 32 kHz oscillator stops running (‘Clk32kProt’ bit)

3.2.2 External supplies control

AB8500 is able to control three external supplies during the start up phase and, when the external supply has this feature, to control LP / HP mode (LP: Low Power mode, device has a reduced current biasing and is able to deliver a reduced current, for example: 100 mA, HP: High Power mode, device has a typical current biasing and is able to deliver its maximum current, for example: 1 A):

- **ExtSupply1Ena**, **ExtSupply2Ena**, **ExtSupply3Ena** balls enable the external supplies.
- **ExtSupply12LPn**, simultaneously controls external supplies 1 and 2 LP/HP modes, **ExtSupply3LPn** controls external supply 3 LP/HP modes.

3.2.3 Start-up sequences

This information is not available in the public domain.

3.2.4 Control interface with DB8500 / AP9500

AB8500 to DB8500 / AP9500 interfaces are the following:

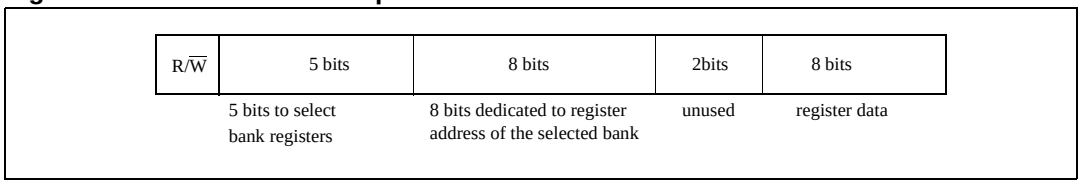
- AB8500 resets DB8500 / AP9500 through the PORDB8500n output ball (active low)
- DB8500 / AP9500 resets AB8500 through the ResetAB8500n input ball (active low)
- DB8500 / AP9500 controls AB8500 through the SPI interface (ApeSpiClk, ApeSpiCsn, ApeSpiDin, ApeSpiDout balls) or through the ApeSCL and ApeSDA balls (see ReguSerialCtrl1 register)
- DB8500 / AP9500 controls the Vmod supply output value delivered by AB8500 through ModSCL and ModSDA balls, this bus is a dedicated bus working up to 10 MHz with the I^2C protocol or through the ApeSCL and ApeSDA balls (see ReguSerialCtrl1 register)
- AB8500 interrupts are sent to DB8500 / AP9500 through IntDB8500n output ball (active low). There are two levels of interrupts, the high level (*ITLatchHier1* to *ITLatchHier3* registers) informs DB8500 / AP9500 in which register the low level interrupt appends. IntDB8500n output ball can be configured as push pull, default, or as open drain through the 'IntDB8500nOD' bit (SystemCtrlSup register).

SPI interface

SPI format

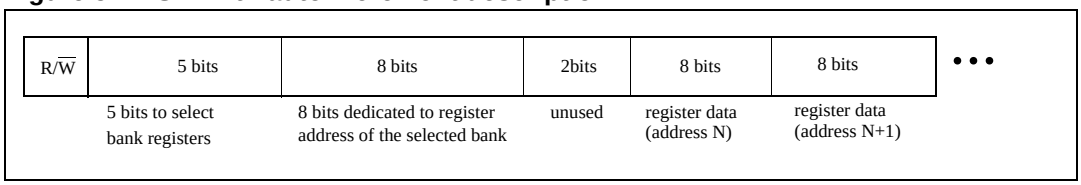
SPI format is a 24 bit frame described in *Figure 4: SPI format description*.

Figure 4. SPI format description



The write operation with auto increment is described in *Figure 5: SPI with auto increment description*

Figure 5. SPI with auto increment description



The detailed information on registers is given in *Section 4: Registers*.

I^2C interface

I^2C™ Modem and PRCMU I2C APE are slave standard/fast serial interfaces compatible with I^2C registered trademark of Philips (version 2.1). These interfaces are standard/fast slave serial interfaces but with a data rate up to 12 MHz (no high speed configuring message needed). The ApeSCL and ModSCL balls are the input clocks used to shift data. The ApeSDA and ModSDA balls are the input/output bi-directional data. xSdA output data are an open drain output ball. The xScl and xSda balls contain pull-up which can be enabled/disabled through 'xSclPupEnaN' and 'xSdaPupEnaN' bits. (*I2CPadCtrl* register)

Device ID

Table 4. Device ID format

b7	b6	b5	b4	b3	b2	b1	b0
AdrID6	AdrID5	AdrID4	AdrID3	AdrID2	AdrID1	AdrID0	R/$\overline{W}$

PRCMU I2C (ApeI2C) device ID is defined as follows:

Table 5. PRCMU I2C device ID

b7	b6	b5	b4	b3	b2	b1	b0
AdrID6	AdrID5	AdrID4	AdrID3	AdrID2	AdrID1	AdrID0	R/$\overline{W}$
0	1	Bank register address					R/$\overline{W}$

Modem I2C device ID is defined as follows:

Table 6. Modem I2C device ID

b7	b6	b5	b4	b3	b2	b1	b0
AdrID6	AdrID5	AdrID4	AdrID3	AdrID2	AdrID1	AdrID0	R/$\overline{W}$
1	0	Bank register address					R/$\overline{W}$

Read/Write operation

Each transaction is composed of a Start condition followed by a number of packet numbers (8- bit long) representing either a device ID plus R/W command or register address or register data coming to/from slave (see *Table 4*, *Table 7* and *Table 8*). An acknowledgment is needed after each packet. This acknowledgment is given by the receiver of the packet. Transaction examples are given in *Figure 6* and *Figure 7*.

Table 7. Register address format

b7	b6	b5	b4	b3	b2	b1	b0
RegADR7	RegADR6	RegADR5	RegADR4	RegADR3	RegADR2	RegADR1	RegADR0

Table 8. Register data format

b7	b6	b5	b4	b3	b2	b1	b0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 6. Read operation

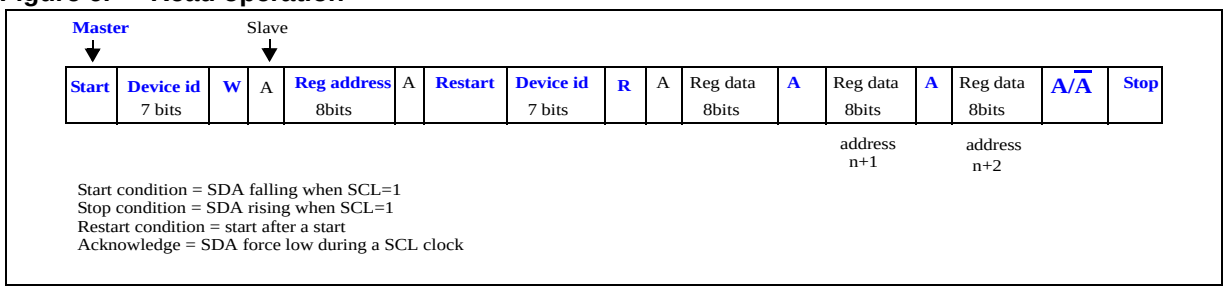
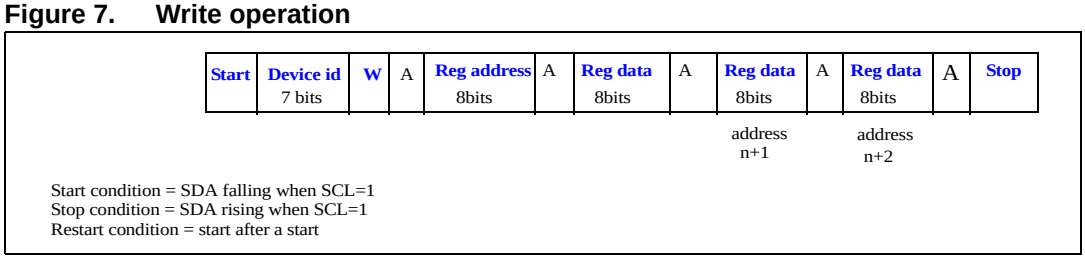


Figure 7. Write operation



3.2.5 PonKey1 and PonKey2 management

This information is not available in the public domain.

3.2.6 Main watchdog

This information is not available in the public domain.

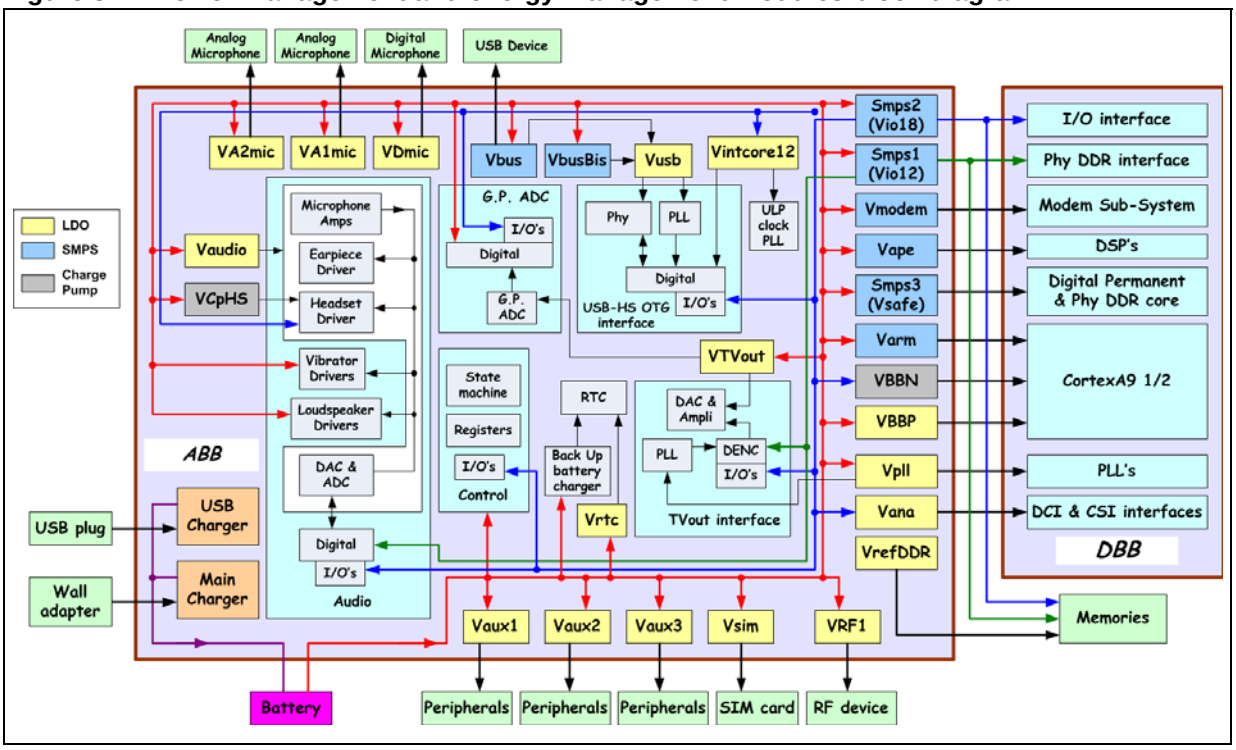
3.3 Clock generator, clock management and RTC

This information is not available in the public domain.

3.4 Power management

Figure 8 gives a general overview of AB8500 power management and energy management used in one of the possible platform configurations, with an external step up and an external step up/down; these two external supplies are optional ones. In this configuration, voltage on the battery can go below 3.2 V, but must stay higher than 2.3 V, (the limit of 3.2 V is linked to the assumption that peripheral supplies by the buck/boost requires a 3 V supply) and the voltage on the Loudspeaker driver stays, independent of the battery voltage, at the same voltage.

Figure 8. Power management and energy management modules block diagram.



To suit different application configurations, AB8500 input supply balls can be connected to different input supply sources, *Table 9* gives the configurations supported by each input supply ball.

Table 9. AB8500 input supply configurations

Ball name	Battery 2.3 to 4.8 V	External supply Max input: 4.8 V	1.8 V SMPS
VbatDig	Yes	No	No
VbatA	Yes	No	No
VinVintCore12	Yes	No	Yes
VinVape	Yes	No	No
VinVarm	Yes	No	No
VinVmod	Yes	No	No
VinVsmps1	Yes	No	No
VinVsmps2	Yes	No	No
VinVsmps3	Yes	No	No
VinVana	Yes	No	Yes
VinVpll	Yes	No	No
VinVBBP	Yes	No	No
VinVBBN	No	No	Yes
VinVaux1	Yes	Yes if Vext > Vaux1+0.2 V	Yes if Vaux1 < 1.4 V
VinVaux2	Yes	Yes if Vext > Vaux2+0.2 V	Yes if Vaux2 < 1.4 V
VinVaux3	Yes	Yes if Vext > Vaux3+0.2 V	Yes if Vaux3 < 1.4 V
VinVRF1	Yes	Yes	No
VinVgauge	Yes	No	No
VinVaudio	Yes	No	No
VinVcphs	Yes	No	No
SmpsVcphs	Yes	No	Yes
VinVDmic	Yes	No	No
VinDclassInt	Yes, these three balls must be connected to the same supply	Yes, these three balls must be connected to the same supply	No
VinVhfR			
VinVhfL			
VinVibraInt	Yes, these three balls must be connected to the same supply	Yes, these three balls must be connected to the same supply	No
VinVib1			
VinVib2			
VinVTVout	Yes	No	No
VinVsim	Yes, if Vbat > Vsim + 0.2 V	Yes	No
VbatVsim	Yes	No	No

3.4.1 DB8500 / AP9500 power supply

Note: These supplies are dedicated to DB8500 / AP9500 and AB8500 devices, no other device can be connected on these supplies.

- **Varm**, step down DC/DC converter to supply the ARM processor. **Varm** supports voltage scaling feature.
- **Vmodem**, step down DC/DC converter to supply Modem sub-system. **Vmod** supports voltage scaling feature.
- **Vape** step down DC/DC converter to supply Smart Video and Audio accelerators and 2D/3D GFx engine.
- **Smps3 (Vsafe)**, DC/DC converter to supply DB8500 / AP9500 permanent digital part and DDR physical interface.
- **Vpll**, LDO to supply DB8500 / AP9500 PLL, **Vpll** also supplies AB8500 27Mhz PLL and ULPClk PLL (analog).
- **Vana**, LDO to supply Camera Serial interface (CSI)/Display Serial interface (DSI) interfaces.
- **VBBN** and **VBBP**, dedicated biasing to optimize DB8500 / AP9500 power consumption versus manufacturing process.

Note: By default, when Vana and Vpll supplies are disabled, a pull down is connected, this pull down can be disabled by the 'VanaDisch' bit (ReguCtrlDisch2 register) and the 'VpllDisch' bit (ReguCtrlDisch register)

3.4.2 AB8500 internal supplies

This information is not available in public domain.

3.4.3 AB8500 supplies for peripherals

These supplies power peripherals such as memories, the camera subsystem, display, sensors, USB device, analog microphones, digital microphones.

- **Vsmps1 (Vio12)**, step-down DC/DC converter to supply all 1.2 V I/Os and memories requiring this supply; its current capability is 1.2 A. Vsmps1 also supplies AB8500 audio and DENC digital parts.
- **Vsmps2 (Vio18)**, step-down DC/DC converter to supply all 1.8 V I/Os and memories requiring this supply; its current capability is 1.2 A. Vsmps2 also supplies AB8500 I/Os and, through the VintCore12 LDO, USB interface digital part.
- **Vaux1, Vaux2** general purpose LDO's to supply peripherals, programmable to 1.1, 1.2, 1.3, 1.4, 1.5, 1.8, 1.85, 1.9, 2.5, 2.65, 2.7, 2.75, 2.8, 2.9, 3, 3.3 V, with a current capability of 200 mA (Vaux1Sel and Vaux2Sel registers).
- **Vaux3** general purpose LDO to supply peripherals, programmable to 1.2, 1.5, 1.8, 2.1, 2.5, 2.75, 2.79, 2.91 V with a current capability of 400 mA (VRF1Vaux3Sel register).
- **VAmic1** and **VAmic2,** LDOs to supply analog microphones. VAmic1 and VAmic2 have a 2.05 V output voltage and their current capability is 5 mA.
- **VDmic**, 1.8 V LDO to supply digital microphones, its current capability is 20 mA.
- **VBUS**, 5 V step-up DC/DC converter supply; USB device able to power a USB device up to 200 mA (300 mA if Battery level > 3V).
- **Vsim**, LDO to supply SIM card. Vsim is programmable to 1.2, 1.8, 3 V, (Reg3-SCTRLRL register) its current capability is 64 mA when supplied by the VinVsim ball.

Vsim can also be supplied through the battery (VbatVsim ball). When supplied by this ball Vsim is able to deliver 64 mA for a 1.8 or 1.2-V output and 1 mA for a 3-V output. The selection between the two supplies is done through ‘VinVsimSupVsim’ bit (Reg3-SCTRLRU register)

Note: When an application is required to work below 3.16 V at battery connection, VinVsim is connected to an external supply able to deliver a voltage supply higher than 3.16V, when an application is not required to work below 3.16 V at battery connection, VinVsim is directly connected to Vbattery.

- **VRF1**, LDO to supply RF transceiver. VRF1 is programmable to 1.8, 2.0, 2.15, 2.5 V, its current capability is 50 mA (VRF1Vaux3Sel register).
- **VrefDDR**, reference supply for DDR memory

Note: By default, when Vaux(i), VDmic, Vsim and VRF1 supplies are disabled, a pull down is connected, this pull down can be disabled by the ‘Vaux(i)Disch’, ‘VdmicDisch’, ‘VsimDisch’ and ‘Vrf1Disch’ bits (ReguCtrlDisch and ReguCtrlDisch2 registers).

3.4.4 Battery-powered features

The following features are directly powered by the battery:

- State machine
- Registers
- Vibrator driver
- Handsfree speaker drivers

Note: Vibrator and handsfree speaker drivers could also be supplied by an external supply (see Table 9)

3.4.5 Internal supply and monitoring

This information is not available in the public domain.

3.4.6 Supply control management

This information is not available in the public domain.

3.5 Energy management

3.5.1 Overview

AB8500 embeds:

- Main Constant Current Constant Voltage (CCCV) charger connected to the wall adapter:
  - Main charger voltage detection
  - Pirate charger detection
  - Switch-mode charging with programmable charging current limits up to 1.5 A.
  - Constant voltage charging with programmable level
  - Thermal protection
  - Reverse polarity protection
  - Dithering when in software mode
- USB CCCV charger:
  - VBUS voltage detection
  - VBUS over voltage detector
  - Switch-mode USB charging with programmable input current and charging current limits up to 1.5 A.
  - Constant voltage charging with programmable level
  - Thermal protection
  - When USB charger is not connected, it is used as 5-V VBUS supply for OTG purposes and is able to deliver 250 mA; out of these 250 mA, 200 mA are dedicated to supply a USB device.
  - Dithering when in Software mode
- Current gauge:
  - Is a 12 bits+sign ADC.
  - The charge and the discharge current of the battery is converted to voltage by an external resistor connected between **GaugeSenseP** and **GaugeSenseN** balls.
  - It is run using 32 kHz clock
  - The integration period is programmable.
- LED indicator

Battery charging functions are designed in order to be compliant with the following standards:

- IEEE1725-2006: standard for rechargeable batteries for cellular phones
- YTD1591: China Communication Standard (Technical requirements and Test Method of Charger and Interface for Mobile Telecommunication Terminal Equipment)
- PSE JISC8714 and JISC8712: Japanese Industrial Standard Committee.
- Universal Serial Bus Specification, Revision 2.0
- USB battery charging specification, rev 1.2 (including ACA support).
- The On-The-Go and Embedded Host supplement to the USB 2.0 specification, Version 2.0

Battery charging can be managed by hardware in the AB8500, a charging algorithm is managed by software through the DB8600/AP9500. As long as the battery voltage has not

reached the VbattOK threshold, fixed by OTP bits, battery charging is controlled by AB8500 (Hardware mode). When the threshold is reached, charging is controlled by DB8500 / AP9500 (Software mode).

Both the main and USB battery chargers are controlled by three control loops:

- Input current limitation
- Output current regulation (CC: Constant Current)
- Output voltage regulation (CV: Constant Voltage)

The input current limitation loop can be used to adjust charging so that the charger voltage does not drop.

To protect the battery, the charger interface embeds:

- A watchdog
- A battery voltage monitoring
- A battery temperature monitoring
- A detection of a non DC charger
- A protection if a charger is wrongly connected in reverse polarity
- Overshoot protection on Vbat during Tx burst

3.5.2 Battery temperature monitoring

This information is not available in the public domain.

3.5.3 Main charger

This information is not available in the public domain.

3.5.4 USB Combo - Charger

This information is not available in the public domain.

3.5.5 LED indicator

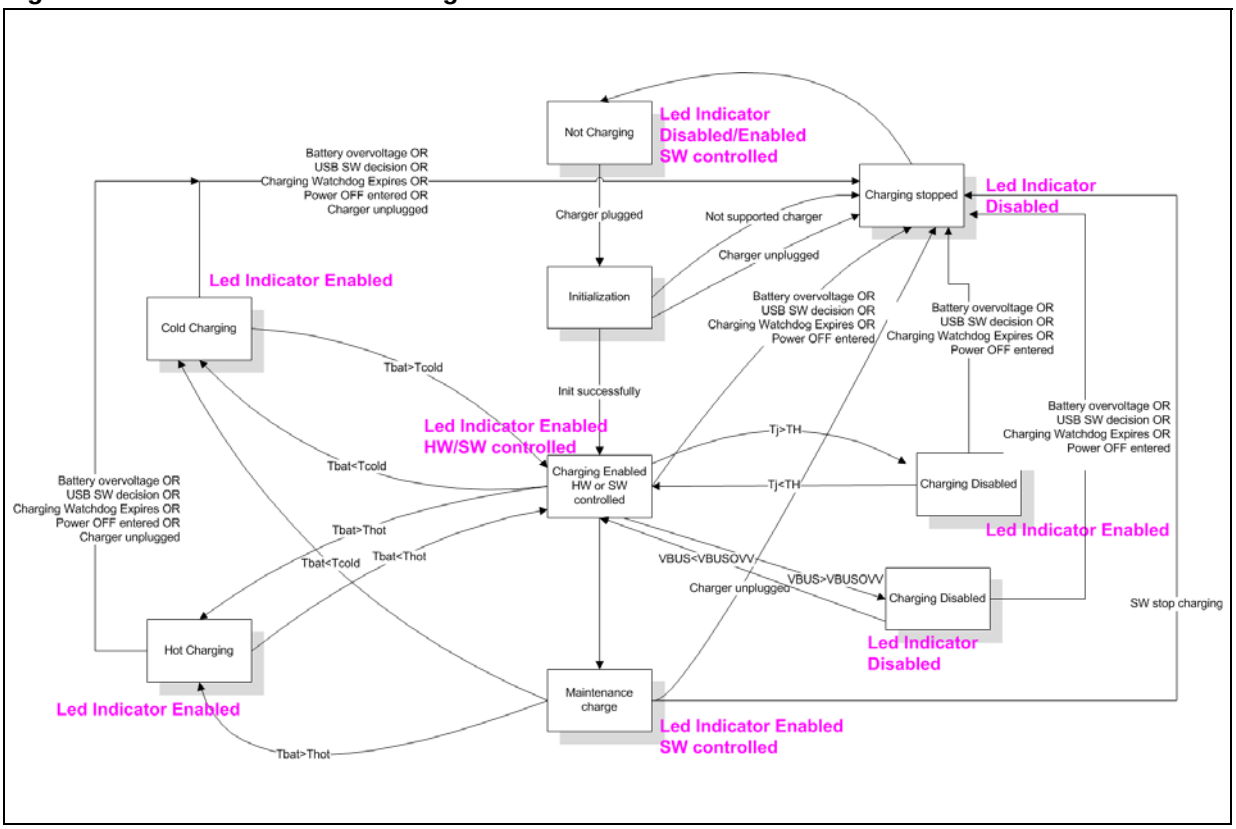
When a main charger or a USB charger is plugged:

- If the AB8500 is in hardware mode:
  - The charging is enabled and the LED indicator is ON, if the LED remains OFF it means that the charger is not valid for battery charging operation.
  - The current LED is set to 2.5 mA
  - The PWM duty cycle is set to 100%
- If the AB8500 is controlled by software through DB8500 / AP9500, the LED indicator is controlled through:
  - LedIndicatorPwmCtrl register for enabling and setting the LED indicator current.
  - LedIndicatorPwmDuty register for setting the PWM duty cycle value, in steps of 1/256. The PWM frequency is 128.5 Hz and is generated from the 32.768 kHz (32.768 kHz/256).

Figure 9 describes the state diagram of the LED indicator when the AB8500 charger is in Hardware mode.

The LED indicator can also be supplied by an external supply, on the condition its voltage is below 4.8 V.

Figure 9. LED indicator state diagram in Hardware mode



3.5.6 USB Combo - Vbus step up

This information is not available in the public domain.

3.5.7 Coulomb counter

This information is not available in the public domain.

3.6 Audio module

3.6.1 Audio module overview

Figure 10 describes the audio module.

The AB8500 audio module is a low power synchronous multi-channel stereo audio codec.

Audio features can be used only if ‘EnAna’ and ‘PowerUp’ bits (*PowerUp* register) are set to “1”.

The AB8500 audio module exchanges audio data through the two digital interfaces at a fixed 48 kHz rate in different formats with up to 8 channels per interface. AudioIF 0 can also operate in burst mode, that means audio data are collected in bursts at high speed through this interface and stored in an internal FIFO, that re-sends the data internally to the Audio macrocell at the correct rate. The audio data interfaces for Analog to Digital (AD) and Digital to Analog (DA) paths can be master or slave.
Digital audio interfaces pins are: FSync0, BitClk0, DA_Data0, AD_Data0, and FSync1, BitClk1, DA_Data1, AD_Data1.

The audio-digital part can handle a maximum of six paths with Channel Filters in each of the AD and DA directions.

In the digital part there are some paths and mixing/multiplexing connections dedicated to special functions:

- Programmable Finite Impulse Response (FIR) filtering at Audio Interface data rate, that can be used for stereo DA path equalizing or AD to DA path sidetone equalizing.
- Simple mixing/multiplexing functions from AD to DA and from DA to AD paths
- Low Latency path for Active Noise Cancellation (ANC) with dedicated Infinite Impulse Response (IIR) and FIR filter. The filters coefficients are constantly updated by DB8500 / AP9500 through the AB8500 control interface.

The audio-digital part also provides inputs for up to six digital microphones and three AD converters (ADC), outputs for four Digital Class-D drivers and three DA Converters (DAC).

The 3 AD converters can support a maximum of two line-in inputs plus a microphone or two microphones plus a line-in input The ADC inputs are, in detail:

- Two switchable analog differential Microphones (Mic1ap, Mic1an, Mic1bp, Mic1bn). Handset microphone and Headset microphone are connected on these inputs. Mic1a and Mic1b inputs cannot be used simultaneously.
- A switchable analog differential input (Mic2p, Mic2n, LinRp, LinRn). These inputs are connected to:
  - Mic2 balls, for an optional auxiliary microphone.
  - LinR balls for an external right stereo source (LinR).
- A Left channel stereo source (LinLp, LinRn) used with LinRp, LinRn inputs when these inputs are selected.

AB8500 analog audio outputs are:

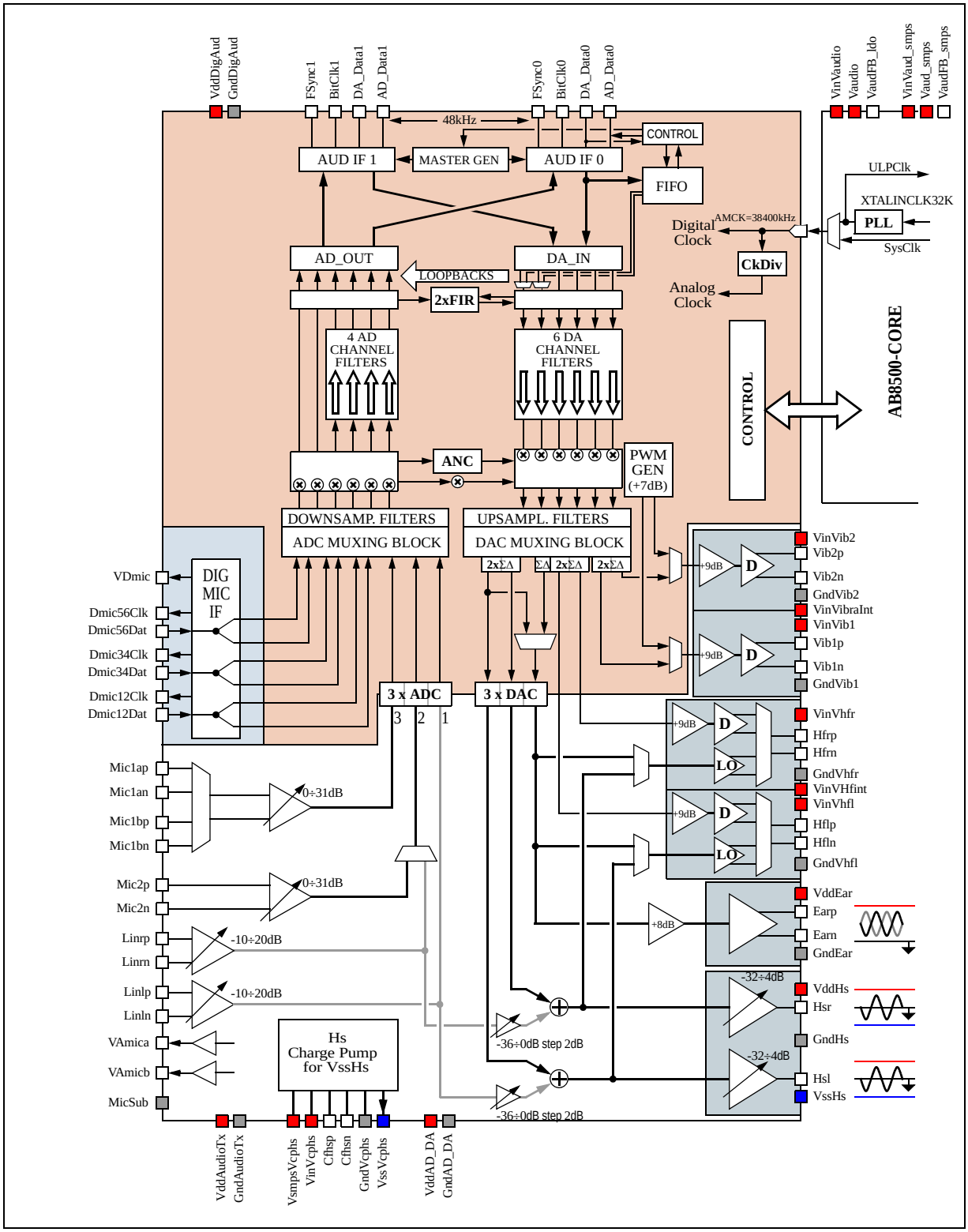
- A stereo headset ear piece (HsR, HsL); left and right ear pieces are connected between the left and right outputs and the ground without a serial capacitor. This stereo output is able to drive a minimum impedance of a 16 Ω ear piece
- A stereo Class D hands free driver/ Class A/B preamplifier (HfRp, HfRn, HfLp, HfLn)
  - When configured as Class D this stereo output is able to drive a minimum impedance of a 6 Ω loudspeaker.
  - When configured as Class A/B its stereo output is able to drive an external mono or stereo amplifier input

    Case 1: it outputs headset stereo channel

    Case 2: it outputs mono external amplifier, in this case it outputs on both the handfree outputs and the earpiece channel.
- A differential ear piece driver (**Earp, Earn**); this output is able to drive a minimum impedance of a 26 Ω ear piece.
- Two differential vibrator drivers (**Vib1p, Vib1n, Vib2p, Vib2n**).The 4 ClassD outputs are divided in stereo Hands-Free outputs (HfL and HfR) plus 2 Vibra Drivers (Vib1 and Vib2)

A fully analog path directly connects a stereo Line-in input to stereo Hs outputs with intermediate gain control.

Figure 10. Block diagram of AB8500 - Audio macrocell



3.6.2 Supply voltage

The Audio Macrocell has many blocks that can be supplied at different voltages. In some cases the block supplies can be joined together to simplify supply network or they can be kept separated to achieve maximum flexibility.

The supply of different blocks of the audio macrocell can be applied and removed in any order without conflicts. The basic rule to follow when applying and removing a supply is that before it is removed, the block must be disabled and it cannot be enabled before its supply is applied.

For example the Ear driver can be enabled only when Vaudio and VddEar are applied (of course other supplies like VddDigAud are also needed), but if the Ear driver is disabled VddEar and Vaudio can be independently applied or removed. At the same time, if only VddEar is not present, all the other blocks under Vaudio can be used.

The Audio control registers are located inside the Digital Audio block and supplied by VddDigAud. Before this supply is removed the content of the registers must be reset to ensure that all blocks are properly shut down. The reset can be done by setting to “1” ‘SwReset’ bit (*AudSwReset* register).

See *Section 3.6.12: Audio module supply options* for details on Hs and Ear supplies.

3.6.3 Audio master clock

The AB8500 audio master clock source can be selected from the 32 kHz clock with an internal PLL, from Ulp clock or from SysClk ball. The master clock frequency is 38400 kHz.

After integer division, this master clock is used to drive internal ADC and DAC converters.

Audio input clock is enabled by ‘AudioClkEna’ bit (SysUlpClkCtrl1 register).

3.6.4 Audio digital Interfaces

The AB8500 exchanges audio data with two separate bidirectional interfaces (AudioIF 0 and AudioIF 1).

At start-up the two audio interfaces are disabled. The eight unused balls are configured as inputs.

The two interfaces work at 48 kHz only with different formats (Time Division Multiplexed (TDM), Left-Aligned). A maximum of 8 channels (slots) for each direction is allowed. The two interfaces can be configured independently in master or slave. AB8500 supports only the 48kHz data rate, that must be derived by an integer division of the 38400 kHz master clock. AudioIF 0 can be configured in a different format for burst data transfer (see *Section : Audio digital interface 0:FIFO and burst mode*).

The maximum configuration for AB8500 is six AD channels (two at 96 kHz, four at 48 kHz) and six DA channels (48 kHz); the two channels at 96 kHz use four slots at 48 kHz. The 96 kHz synchronism is created from 48 kHz sync with Bit Clock.

The Frame Sync and Bit Clock polarity can be inverted with bits ‘FSync0P’, ‘BitClk0P’ ‘FSync1P’, ‘BitClk1P’ (*DigIFConf2* and *DigIFConf4* registers)

Note: *In all the figures below the format descriptions and the timings always assume that the polarities are not inverted (all polarity bits set to zero, default state).*

Each interface has an AD_Data (output) and a DA_Data (input) ball; however this is only their suggested direction because their use can be inverted or they can be both used as

inputs and outputs. Each interface can be connected to multiple devices, because it supports tristate mode in every slot.

The audio interfaces can be configured with different data word lengths, 16, 20, 24 or 32 bits per word; however a maximum of 24 bits is actually processed. If more than 24 significant bits are provided at the input, then a truncation to 24 bits is performed. Output words of more than 24 bits are 0-padded.

Depending on the selected data interface format (TDM and Left-Aligned) an excess number of bit clock periods at the end of the last slot of a frame is ignored.

Audio digital interface: TDM format

The TDM format supports up to eight channels (slots) per frame. The slots have a length defined by bits ‘IF0WL[1:0]’ and ‘IF1WL[1:0]’ (*DigIFConf2* and *DigIFConf4* registers), all the slots are packed one next to the other, extra bits at the end of the last frame are ignored.

The TDM format can also be configured to be compatible with the PCM format

The enabling of the master clock, the Fsync(i), the BitClk(i) and the over sampling frequency of BitClk(i) are set through the*DigIFConf1* register.

Figure 11. AudioIF: TDM format, 8 channels, Delayed, 32 bits Word Length

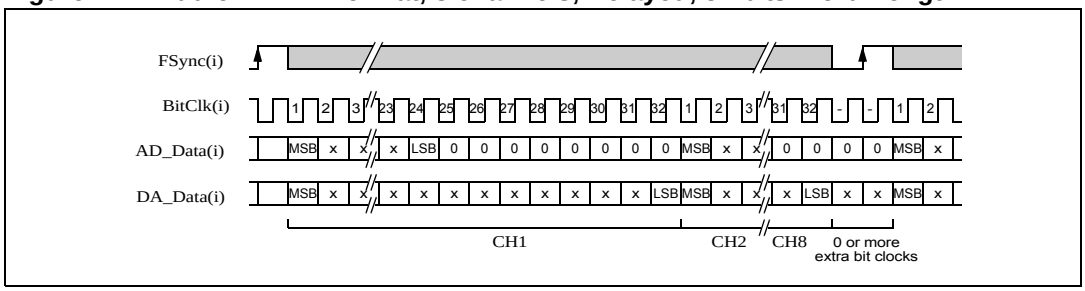
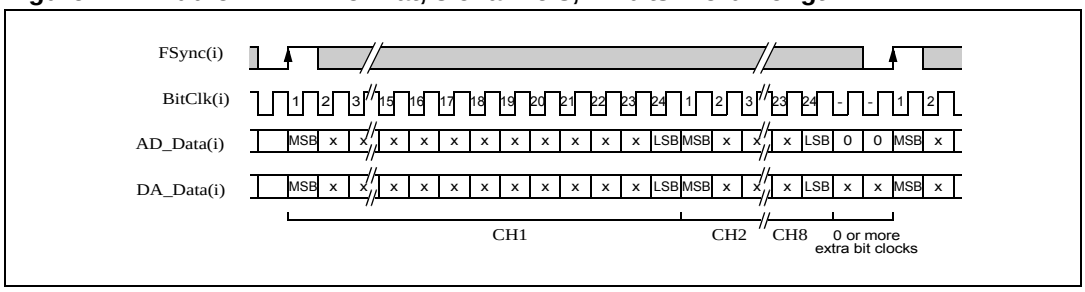


Figure 12. AudioIF: TDM format, 8 channels, 24 bits Word Length



Note: The FSync(i) duty cycle in master mode is 50%.

Audio digital interface: left-aligned format

The Left Aligned format supports up to two channels (slots) per frame. The slots have a length defined with bits ‘IF0WL[1:0]’ and ‘IF1WL[1:0]’ (*DigIFConf2* and *DigIFConf4* registers). The first slot is aligned with the rising edge of FSync(i) and the second is aligned with the falling edge of FSync(i) (when FSync polarity is not inverted). Extra bits at the end of each slot are ignored.

Note: TDM or Left-aligned format is selected through the ‘IF(i)Format[1:0] bits, delayed or non delayed format is selected through the ‘IF(i)Del’ bits (DigIFConf2 and DigIFConf4 register).

Figure 13. AudioIF: Left aligned format

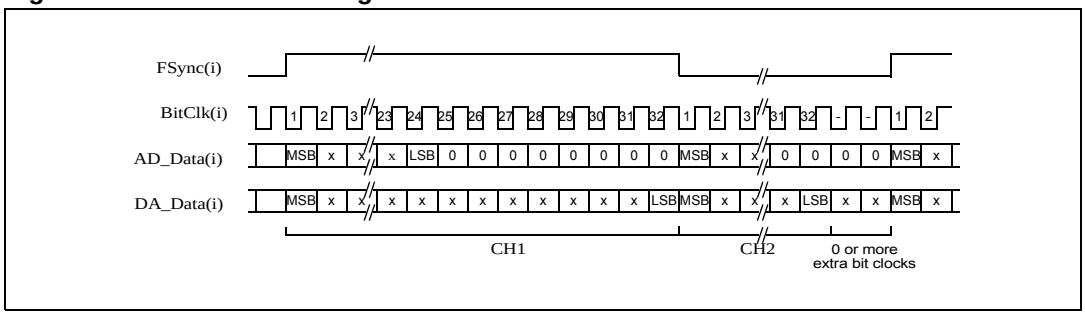
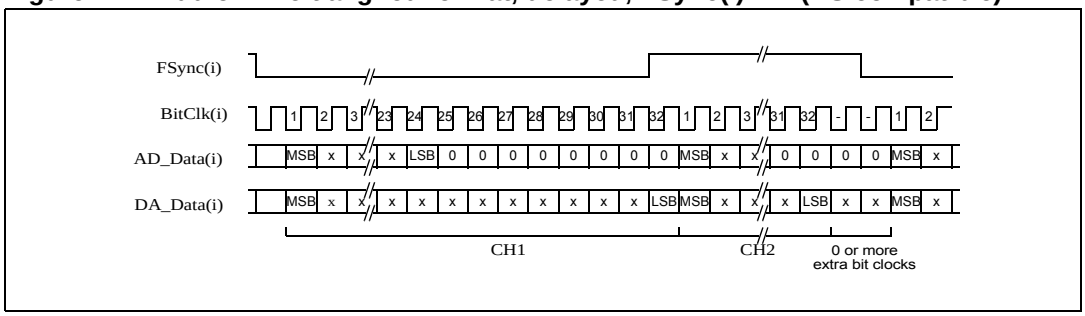


Figure 14. AudioIF: Left aligned format, delayed, FSync(i)P=1 (I^2S compatible)



Audio digital interface 0:FIFO and burst mode

When configured in Burst Mode (see the *DigIFConf3* register, and the *FIFOConf2* register) the AudioIF0 signals change functionality and digital audio data is sent through the interface in blocks and stored in an internal FIFO, then the interface is stopped until the FIFO becomes empty. In this paragraph the definition “Normal Mode” refers to any IF format other than Burst. Burst Mode is designed to work together with a compatible digital audio data source, in this case the DB8500 / AP9500 Application Processor

The burst mode interface format is left-aligned 2 channels 20 bits delayed. The BitClk0 ball, programmable to 38.4 or 19.2 MHz clock, through the ‘BFIFO19M2’ bit (*FIFOConf1* register), runs only during the burst, in addition the FSync0 ball will toggle only during burst transfer. Note that in Burst Mode, the word length is always 20 bits and cannot be programmed as for other formats.

The Burst Mode control and FIFO configuration is done mainly through two control registers, one (‘BFIFOTx[7:0]’, *FIFOConf2* register), used in master mode only, that controls the burst length from 0 to 1536 samples (32 ms), in steps of 8 samples, and the other (‘BFIFOInt[5:0]’, *FIFOConf1* register) that selects the FIFO threshold (from 0 to 512 samples, step 8 samples) below which a data request is generated.

When AB8500 is configured in Burst Mode the generation of a data request to wake up the DB8500 / AP9500 is done with a rising edge of the AD_Data0 ball, then the DB8500 / AP9500 will start the burst (length controlled by DB8500 / AP9500 in Slave, and by bits ‘BFIFOTx[7:0]’ in Master). *Figure 17.*-shows an example of data request with consequent start of the burst. The Data request with ball AD_Data0 can be masked setting ‘BFIFOMask’ = 1 (*FIFOConf1* register).

When the interface is configured as Master the switch between Normal and Burst Mode can be done on the fly: first the frame number on which the change will occur must be programmed on bits ‘BFIFOFramSw[7:0]’ (*FIFOConf4* register), then bit ‘IF0BFifoEn’ (*DigIFConf3* register) must be set to 1 to enable the seamless change. The internal 11 bits

frame number (FN) counter starts at the enable of the interface in Normal Mode and is compared to 8*'BFIFOSample[7:0]' bits (*FIFOConf6* register). If the 'IF0BFifoEn' bit is set to 1 before the interface is active then IF0 will start in burst mode and 'BFIFOFramSw[7:0]' will be ignored.

If Master configuration is chosen, then bit 'BFIFOMast' (*FIFOConf3* register) must be set to "1". After all FIFO level and response time configurations are set the bit 'BFIFORun' (*FIFOConf3* register) will enable the start of the burst mode. Note that the bit 'BFIFORun' is an asynchronous FIFO enable, as it enables/disables all the clocks to the burst FIFO block, while 'IF0BFifoEn' acts as a synchronous enable, because, when it goes to "1" it cleanly starts the burst mode, and when it goes to "0" the system waits for the end of the burst to stop.

In Burst Mode it is possible to insert dummy slots after the first two active ones. Bits 'BFIFOExSl[2:0]' (*FIFOConf3* register) control the number of added dummy slots. At the end of the first burst transmission the DB8500 / AP9500 goes to power down and the interface stops. When a new burst transfer is needed a wake up is generated to the DB8500 / AP9500 with a rising edge of the AD_Data0 ball. The burst transmission starts with a programmable delay of 26.7 µs*'BFIFOWakeUp[7:0]' (*FIFOConf5* register).

The switch from burst to normal (IF0BFifoEn=0) happens when the FIFO is empty.

In some cases there can be the need to have some extra bit clocks that precede and follow a data burst to properly communicate with the digital audio data source. The number of bit-clocks can be configured with 'PreBitClk[2:0]' bits (*FIFOConf3* register)

The examples below show the switch between normal and burst mode in the particular case of I^2S interface. The same figures are valid for other TDM configurations.

Figure 15. Switch between normal and burst modes (Master)

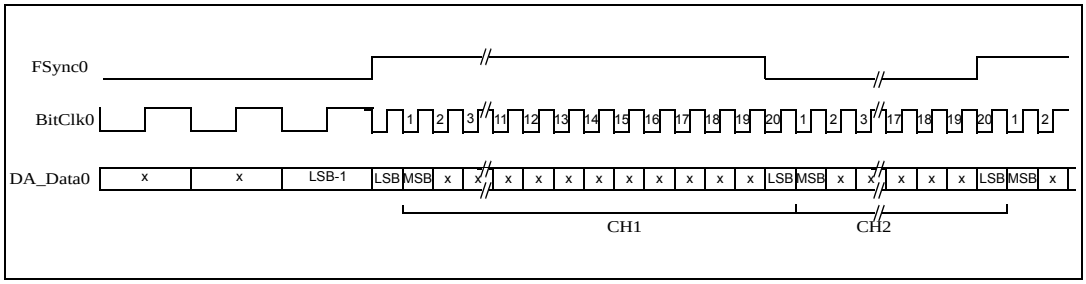


Figure 16. Switch between burst with 2 pre-frame bit clocks and normal mode

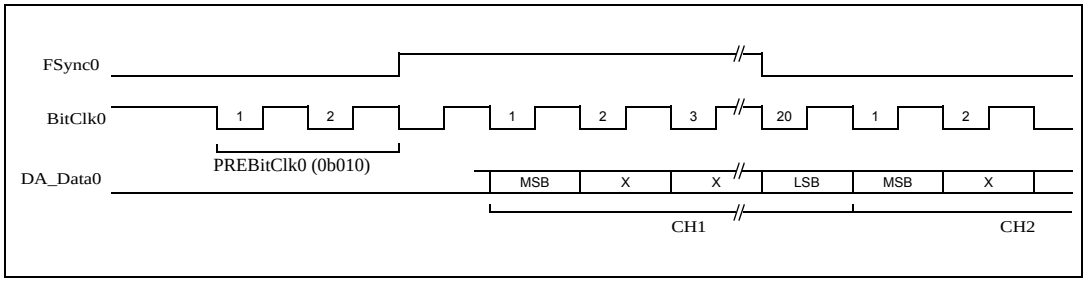


Figure 17. AudioIF 0 in burst mode, start of a single burst

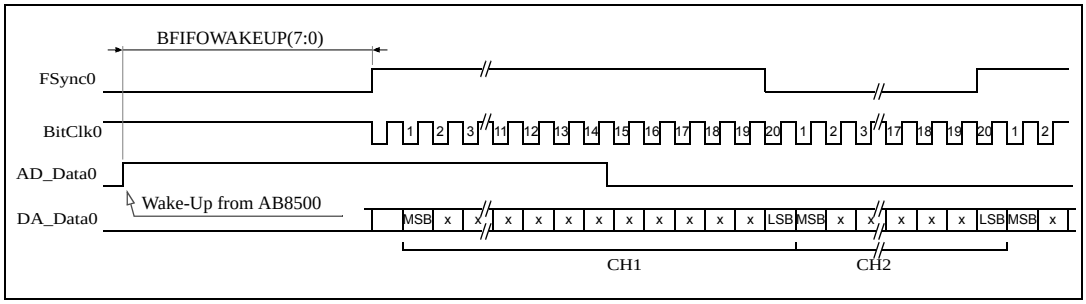


Figure 18. AudioIF 0 in Burst Mode. Start of a single burst with 3 pre-frame bit clocks

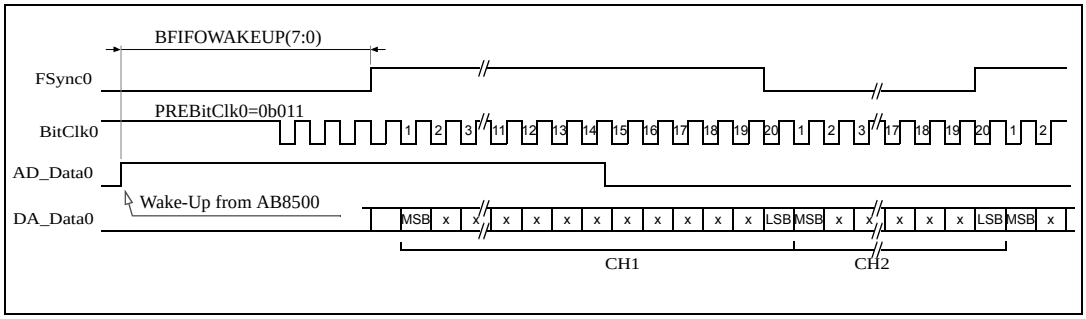
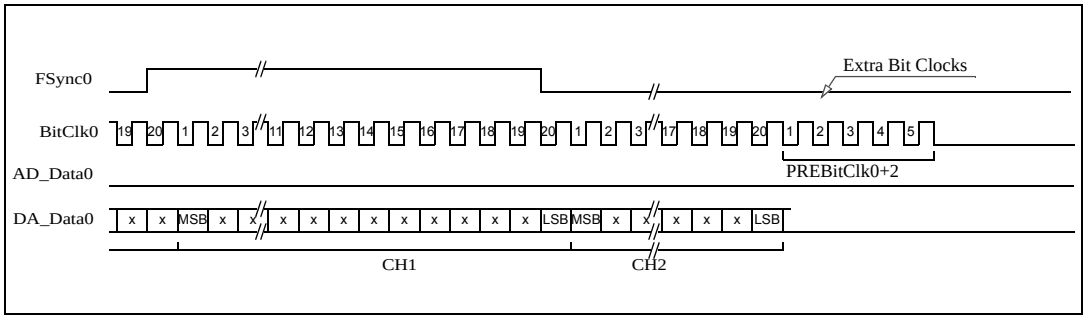


Figure 19. AudioIF 0 in Burst Mode. End of a burst



Audio digital interface: master generators

The two Digital Audio Interfaces, through ‘IF(i)Master’ bits (*DigIFConf3* register) can be driven in Master Mode by two Master Generators. The interface formats can be different in AudioIF0 and AudioIF1 but the data rate is always 48 kHz. When both interfaces are configured in master mode they have identical FSync.

The bit clock is a multiple of 48 kHz and it can only be:

- 1.536 MHz (up to 2 channels, 16 bits/ch at 48 kHz)
- 3.072 MHz
- 6.144 MHz
- 12.288 MHz (up to 8-channels, 32-bits/ch at 48 kHz)

The bit clock periods are uniformly spread inside the Fs period.

Audio digital interface: bypass mode

It is possible to internally connect the two digital audio interfaces with a direct bypass to allow devices not connected to the same IF to communicate.

The bypass function is active also when the ‘Power-Up’ bit is set to 0 (*PowerUp* register), but the digital audio supply must be present to enable the audio control registers.

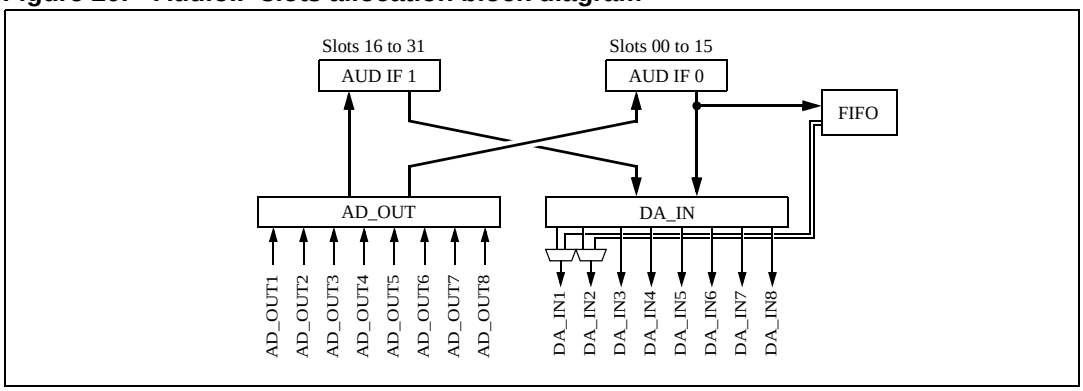
The bypass can be activated separately on data and on frame and bit clocks. The bypass function is controlled with bits ‘IF0DatatoIF1AD’ ‘IFOClkToIF1Clk’, ‘IF1DatatoIF0AD’ ‘IF1ClkToIF0Clk’ (*DigIFConf3* register).

Audio digital interface: slots allocation

The digital audio interfaces can internally exchange data connected with up to six channels in each direction, so that the slot of the interface can be associated with the internal channels. See from *ADSlotSel1* register up to *ADSlotSel16* register and from *DASlotConf1* register up to *DASlotConf8* register for all the available combinations.

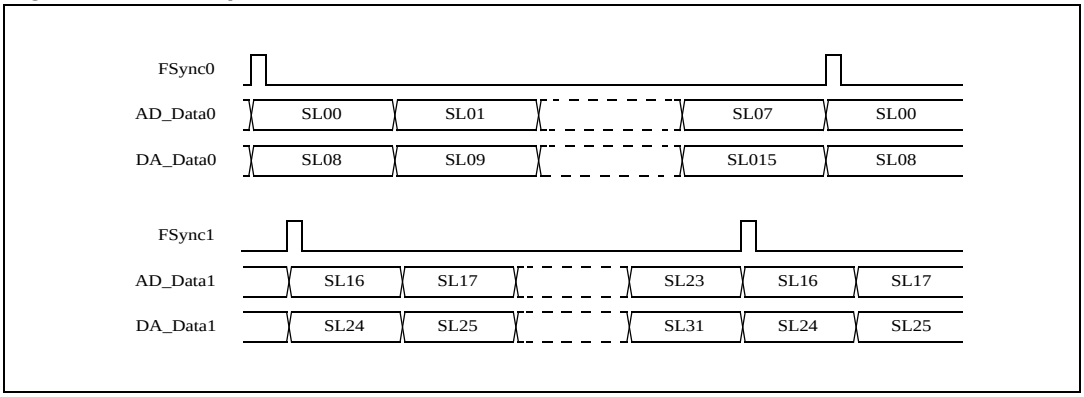
In the AD path, some channels exchange data at 96 kHz (AD_OUT5 and AD_OUT6) while the interfaces can run only at 48 kHz, so two slots are needed in each frame to properly operate.

Figure 20. AudioIF slots allocation block diagram



The fixed slots positions of the two audio data interfaces are described as follows:

Figure 21. Slots position in AudioIF



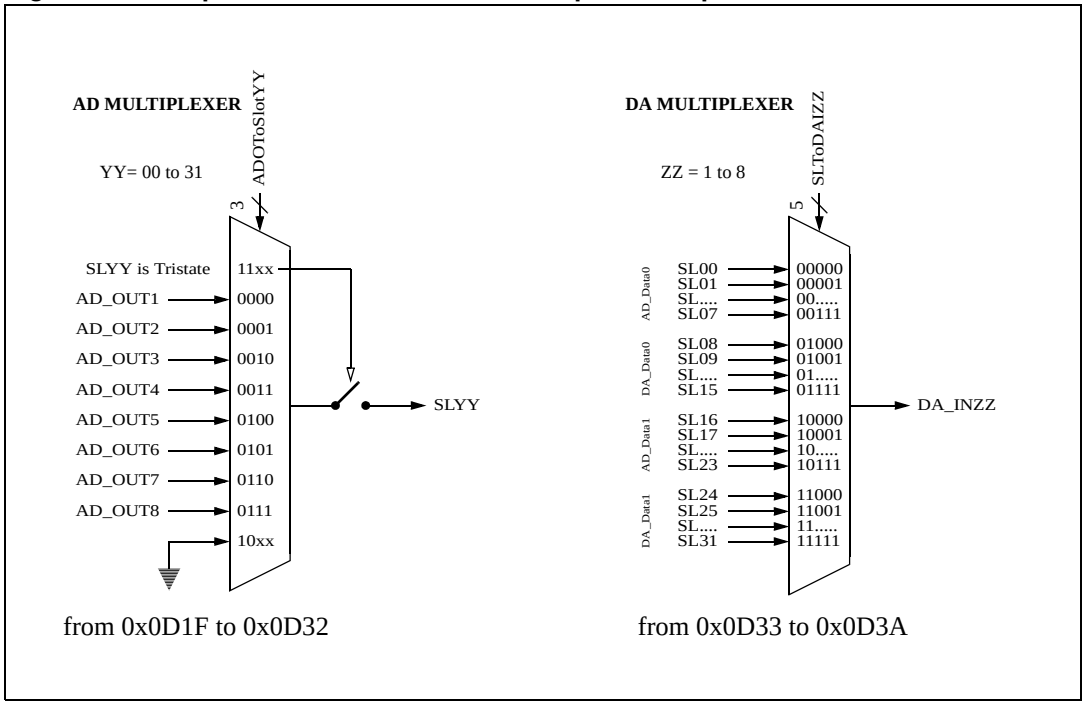
In case one interface is configured with less than eight slots, then some of them can be missing: if AudioIF0 is configured in Left-Aligned format, two channels only, then slots SL02-07 and SL10-15 will be missing.

The two audio interfaces exchange AD data with the eight channels AD_OUT outputs (four 48 kHz plus two 96 kHz channels) of the digital AD paths. AD paths are enabled through ‘EnAD(i)’ bits (*ADPathEna* register). One AD multiplexer is associated to each of the 32 slots. To be able to handle the 96 kHz data two output paths are associated to AD5 and AD6 channels: AD_OUT5/7 is associated with the 96 kHz AD5 channel, while AD_OUT6/8 corresponds to AD6.

The AD Multiplexer also selects the slot output state (‘ADOToSlot(i)[3:0]’ = 11xx means that slot (i) is tristate). This allows the interface to be connected to more than one external device. See from *ADSlotSel1* register up to *ADSlotHizCtrl4* register for all the AD available combinations.

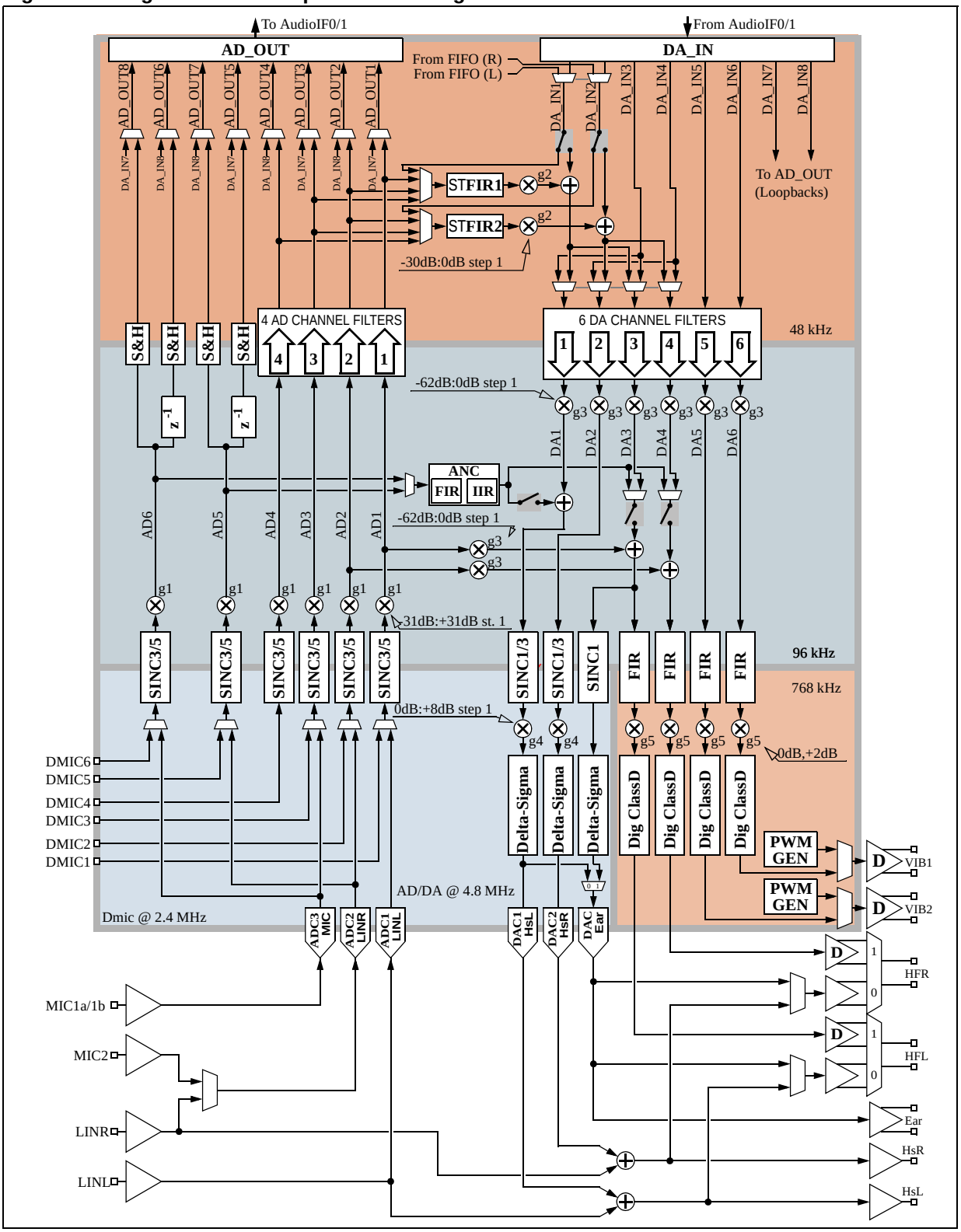
On the DA path, the eight inputs of DA paths (DA_IN1:8), DA_IN1 up to DA_IN6 are enabled through ‘EnDA(i)’ bits (*DAPathEna* register) and all paths can get data from any slot, so one DA multiplexer is associated with each DA_IN input. See from *DASlotConf1* register up to *DASlotConf8* register for all the available DA combinations.

Figure 22. AD path to Slots and Slots to DA path multiplexers



3.6.5 Digital AD and DA paths

Figure 23. Digital AD and DA paths block diagram



AB8500 can handle up to six AD channels and six DA channels simultaneously. Two AD channels work at 96 kHz data rate and four AD plus six DA channels work at 48 kHz.

AD and DA channel filters

The AD and DA paths perform channel audio filtering, selectable among audio and voice responses, for AD, ‘AD(i)Voice’ bits (*ADFiltConf* registers), for DA, ‘DA34Voice’ and ‘DA56Voice’ bits (*DASlotConf3* and *DASlotConf4* registers). Audio filters are designed to provide maximum flat band response with steep cut-off, while voice filters have an 8 kHz bandwidth with a softer low pass filter but with very low group delay. The channel filters responses are fixed, so they cannot be used for equalizing audio data. Their purpose is to avoid aliasing in the oversampled ADCs and DACs.

Digital paths: mixing and multiplexing features

The AB8500 includes some digital mixing and multiplexing features. *Figure 23* shows all path connection possibilities.

In the AD path every Dmic(i) input is always connected to AD(i) channel, while the analog inputs, through ‘AD(i)Sel’ bits (*DigMultConf1* register) can be multiplexed in different ways. Depending on the latency constraints or needed performance, the SINC filters order can be configured. When DMIC inputs (typically 4th order modulated signals) are used a SINC5 or SINC3 filter can be selected through ‘Dmic(i)Sinc3’ bits (*DmicFiltConf* register).

Digital microphones 1 to 4 can also be used in parallel in order to achieve, through signal post-processing (not done in AB8500), microphone directionality.

In the DA path every one of the 6 channels is always associated to a specific output driver: DA_IN1 to DA_IN6 respectively to the HsL, HsR, HfL, HfR, Vib2, Vib1. The Ear output can share the channel with HsL (DA_IN1) path, ‘DA3ToEar’ bit (*DmicFiltConf* register); note that in this case the Ear output should not be used together with the Hs outputs. Alternatively the Ear output can be connected to the DA3 (HfL) path. If low latency is required, SINC filters on DA paths 1 and 2 can be configured to first order through ‘HsSinc1’ bit (*HsLEarDigGain* register). In DA paths 3 to 6, the FIR filters can be configured as SINC1 to minimize latency.

Stereo programmable FIR filters are available for mixing AD path signal with DA path (sidetone function) or for DA path equalization (*SidFIRAdr*, *SidFIRCoef1*, *SidFIRCoef2*, *SidFIRConf* registers). Through ‘FIRSid(i)Sel[1:0]’ bits (*DigMultConf2* register) the FIRs can be used as single channel for voice application or for more complex stereo path equalization. The FIRs coefficients can be updated on the fly while audio data is flowing.

A low-latency connection at a 96 kHz rate from AD path to the DA path is done to implement Active Noise Cancellation (ANC).The ANC signal obtained from microphones is used to cancel external noise in two ways: through ‘DAToHfR/LEn’, ‘HfR/LSel’ bits (*DigMultConf2* register), it can be mixed with the RX path and sent to the Ear output or it can be independently sent to the HF speakers to be acoustically added to the Ear output. The ANC block consists of a sequence of IIR and FIR filters with coefficients that are programmable through the AB8500 control interface (*ANCConf1* register up to *ANCConf4* register).

The last connection from the AD to the DA paths is implemented to connect the stereo line-in path to digital classD Hands-Free (HF) output, the gain of these paths is set through ‘AD(i)LBGain[5:0]’ bits, a fading effect can be enabled through ‘FadeDisAD(i)L’ bits (*ADDigLoopGain1* and *ADDigLoopGain2* registers).

Anti-click feature in digital gain controls

A built-in anti-click feature that avoids audible effects for big gain changes is present in G1, ‘ADDigGain(i)[5:0]’ bits (*ADDigGain1* register up to *ADDigGain6* register), G2, ‘FIRSid(i)Gain[4:0]’ bits (*SidFIRGain1* and *SidFIRGain2* registers), G4, ‘HsL/RDGain[3:0]’ bits (*HsLEarDigGain* and *HsRDigGain* registers), gains are described in *Figure 23*. When in a register with gain=GA a new value gain=GB is set, the actual gain is not applied immediately but in steps of 1dB, starting from GA to arrive to GB. If enabled through ‘FadeDis(xxx)’ bits, part of the same register as for G1, G2, G4 gains, every step is applied for approximately 1 ms (selectable with ‘FadeSpeed[1:0]’ bits (*HsRDigGain* register) and the step is applied in the presence of a signal zero-cross. This feature can be disabled individually for each gain if a specific gain value needs to be applied immediately.

The DA(i) path gains are set through ‘DA(i)Gain[5:0]’ bits, a fading effect can be enabled through ‘FadeDisDA(i)’ bits (*DADigGain1* to *DADigGain6* registers).

3.6.6 AD converters and analog inputs

The analog microphone and line amplifiers:

- Are enabled through the ‘EnMic(i)’ and ‘EnLinR/L’ bits
- Are muted through the ‘MutMic(i)’ and ‘MutLinR/L’ bits (*AnaConf2* register).

The analog microphone amplifiers (*AnaGain1* and *AnaGain2* registers):

- Can be put in low power mode through the ‘LowPowMic(i)’ bits
- Microphones can be connected in single ended through the ‘EnSEMic(i)’ bits

The three independent ADCs are enabled through the ‘EnADCMic’, ‘EnADCLinL/R’ bits, they can be connected respectively to one analog microphone, selected from two through the ‘Mic1Sel’ bit, one line-in or 1 Mic through ‘LinRSel’ bit (*AnaConf3* register), and 1 line-in.

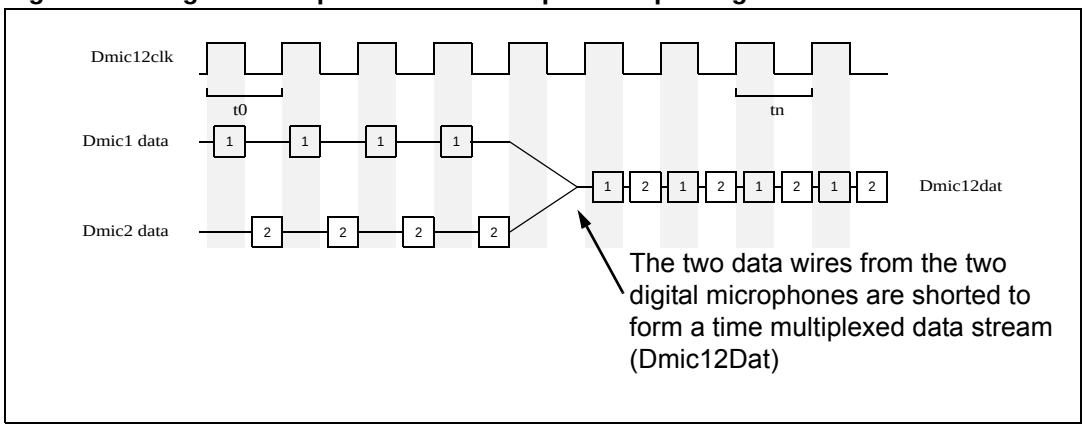
The microphones inputs are optimized for low level signals and provide a high signal to noise ratio with high input gain and a constant input resistance of 200 kΩ. The Microphone inputs gain range is from 0 to +31 dB step 1dB (‘Mic1Gain[4:0]’ and ‘Mic2Gain[4:0]’ bits of *AnaGain1* and *AnaGain2* registers).

The line-in inputs are optimized for high level signals and provide 92 dB of signal to noise ratio at <=0 dB gain and better than 90 dB SNR with <=12 dB gain. The input resistance is 24k Ω. The Line-in inputs gain range is from -10 to +20 dB, step 2 dB (‘LinL/RGain[3:0]’ bits of *AnaGain4* register.

3.6.7 Digital microphones inputs

Up to six digital microphones (three stereo) can be connected to AB8500. Microphone digital paths are enabled through the ‘EnDmic(i)’ bits (*DigMicConf* register). Every stereo digital microphone input shares a single wire to send data to the Dmic input (Dmic12dat, Dmic34dat or Dmic56dat). AB8500 provides a 2400 kHz clock needed to run each interface.

Figure 24. Digital microphones 1 and 2 input multiplexing



The input data from the digital microphones is a time multiplexed stream formed by two Pulse Density Modulated (PDM) signals (up to the fourth order modulation) that alternate data with high-impedance state. The two streams are separated inside AB8500 Audio macrocell. It is assumed that samples one and two of the same time-slot t_n in *Figure 24* are sampled at the same time, therefore they are also time-aligned inside AB8500.

The Digital Microphone input is also compatible with a single digital microphone that does not support high impedance state.

The Digital microphone inputs accept sigma-delta modulated 1-bit input data, with a maximum of fourth order noise shaping.

When 0 dB gain is applied at DMIC mixer input, the digital input path does not saturate for inputs that show all-ones or all-zeros streams: the all ones input stream corresponds to the maximum digital positive value and the all-zeros corresponds to the minimum digital negative value.

Digital Microphones Supply: VDmic

A dedicated LDO (**VDmic** ball) is available to supply all the external digital microphones. This LDO is enabled by the ‘VdmicEna’ bit (VaudioSupply register).

3.6.8 Analog and digital microphones digital gains

The digital gains of analog and digital microphones, have a different full scale alignment.

When 0 dB gain is applied at the analog microphone input, a full-scale analog input signal is converted to a full-scale digital output signal. (0 dbV_{rms} input with 0 dB gain corresponds to 0 dBFS).

When 0 dB gain is applied at the digital microphone mixer input an all-ones or all-zeros input signal is converted to a full-scale digital output signal, that means that a typical 1-bit modulated input stream that contains a -6 dB signal (which is typically the maximum signal before heavy distortion) will be converted to a -6dBFS digital output signal.

3.6.9 Analog microphone bias

The AB8500 Audio macrocell includes two low-noise Microphone Bias circuits at 2.05 V, VAmic1 and VAmic2, activated by the ‘Vamic1/2Ena’ bits of the VaudioSupply register. When inactive, the Microphone Bias outputs can be in High impedance or they can be

pulled down, less than 1 kΩ resistance, through ‘Vamic(i)_dzout’ bits (ReguCtrl1VAmic register).

Note: The Microphone Bias circuit is supplied directly from the battery and it can be active when all of the audio macrocell, including its supply voltages, is powered down. This allows the external microphone push-buttons and dedicated circuits to be supplied so that an interrupt request can be generated by user request.

3.6.10 Analog paths

An analog path is provided in the audio macrocell to connect the line-in stereo inputs directly to the headset drivers (typical application is analog FM radio listening feature). The analog path can also be mixed with DAC signals. This path is enabled through path gain control bits ‘LinToHsLGain[4:0]’ (*DigLinHsLGain* register) and ‘LinToHsRGain[4:0]’ (*DigLinHsRGain* register). A dedicated -36 dB to 0 dB step 2 dB range attenuation is available.

Note: When this path is used the bits ‘EnDrvHsL’ and ‘EnDrvHsR’ (*AnaConf3* register) *must be enabled.*

3.6.11 Output drivers and negative charge pump

One DA Converter for each analog output driver (two for Headset and one for Ear) is present in the AB8500 Audio macrocell. The DAC path gain is mainly controlled in the digital domain, with extra gain regulation available only at Headset (Hs) output stage.

Four class-D output drivers, two Hands-Free (HF) and two Vibra (Vib), are driven through four independent digital PWM signals. Alternatively to the HF class-D drivers, two line-out signals can be provided. The line-out signals are not independent but they rely on the 3 available DACs.

The maximum number of output channel usable together is six and it corresponds to the number of channel handled by the digital.

Ear analog power output

The Ear driver is enabled with the ‘EnEar’ bit (*AnaConf4* register) and its corresponding DAC with ‘EnDACEar’ bit (*DAPathConf* register), it can be muted through ‘MutEar’ bit (*MuteConf* register). The Ear driver and the Ear DAC can be put in low power mode through ‘EarDrvLowPow’ and ‘EarDAClowPow’ (*AnaConf1* register). The digital DA path that provides the audio data to the Ear driver can be selected between DA1 and DA3 by bit “DA3ToEar” (*DmicFiltConf* register)

The Ear driver has a built-in short-circuit protection feature that is enabled by default. If a short is detected during operation an interrupt request is generated, ‘IT_ShortEar’ bit (*AudIntSource1* register); if ‘EnShortPWD’=1 (*ShortCirConf* register) the driver is automatically disabled. In order to re-enable the driver the ‘EnEar’ bit must be set to “0” and back to “1” again. The automatic shutdown of the drivers can be disabled, ‘EnShortPWD’=0, allowing only an IRQ request. The short circuit protection can be disabled with ‘EarShortDis’ bit (*ShortCirConf* register).

The Earpiece driver has a separate external power supply (VddEar) that must be greater than or equal to VddAD_DA. This external supply can be switched off without any problem if the driver has been disabled in advance. The PSR of VddEar makes it suitable for a direct connection to the battery. See *Figure 26* for an example of Ear driver supply connections.

Through the ‘EarSelCM[1:0]’ bits (*AnaConf1* register), the Earpiece driver has a programmable output common mode voltage to be able to provide the maximum output power depending on its supply voltage.

When the Ear driver is disabled, there is a 25 kΩ resistance between **Earp** and **Earn** balls with a floating common mode value between ground and VddAD_DA.

Figure 26 shows the different way to supply the earpiece driver

Headset Analog power outputs

The headset, HsL and HsR, drivers have dedicated enable bits, ‘EnDrvHsL’ and ‘EnDrvHsR’ (*AnaConf3* register) and ‘EnHsL’, ‘EnHsR’ bits in (*AnaConf4* register) to allow independent enable for analog paths, while the corresponding DACs are enabled with ‘EnDACHsL’ and ‘EnDACHsR’ bits (*DAPathConf* register).

Headset Anti click and Zero Cross Detection (ZCD)

The headset drivers provide a built-in click reduction system at power up/down and for gain change.

The best power up sequence is to first enable all of the path chains before the Headset drivers and then set the ‘EnHsL’ and ‘EnHsR’ bits to “1”. If the ‘MutHsL’ and ‘MutHsR’ bits (*MuteConf* register) are set to “1” then after startup the Headset drivers will be muted, otherwise they will first startup muted, then they will change the gain from the lowest value to the programmed one using all intermediate steps. The step duration is programmable through ‘HsFadSpeed[1:0]’ bits (*DigMicConf* register) and the actual gain change occurs within the programmed duration only at the input signal zero-cross.

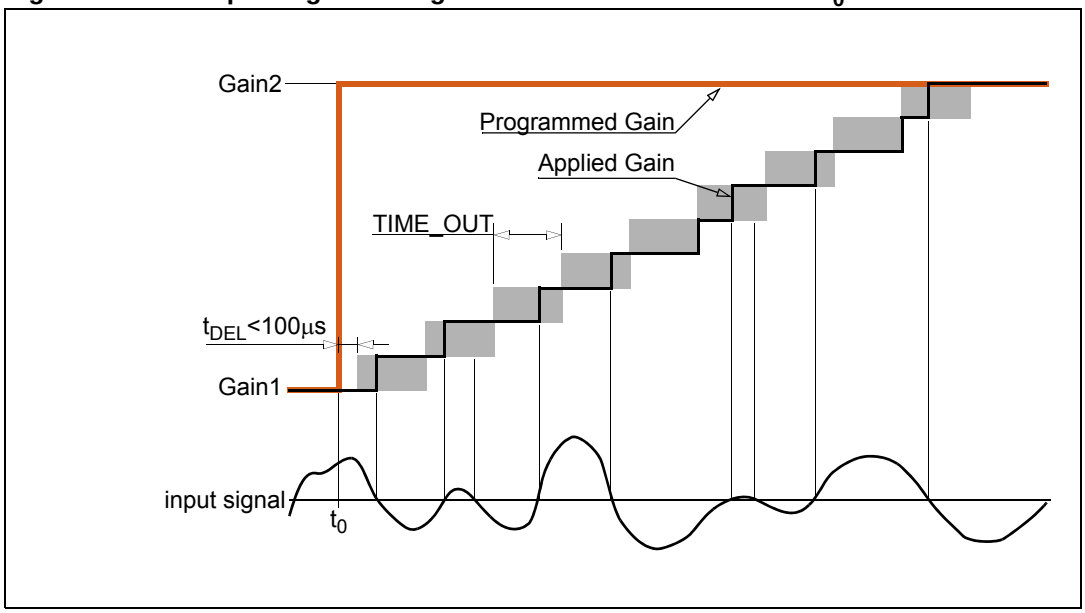
An analog gain from -32 dB to -20 dB, step 4 dB and -20 dB to +4 dB, step 2 dB is programmable on headset drivers through ‘HsLGain[3:0]’ and ‘HsRGain[3:0]’ (*AnaGain3* register). Every gain change will automatically go through all the available intermediate steps and with zero cross detection. Headset fading and zero crossing detection features can be respectively disabled through the ’HsFadDis’ and ‘HsZcdDis’ bit (*ShortCirConf* register).

When the headset driver is muted or powered down the gain is changed from the current one to the minimum with all the intermediate steps and after the sequence the actual mute/power-down occurs.

Through the ‘HsHpEn’ bit (*AnaConf1* register), a high-pass filter is selectable in the headset drivers to remove full path offset.

All the features described above can be disabled to obtain full control and maximum speed in operating the driver. All the functions are also available for the analog path without the need of a system clock.

Figure 25. Example of gain change from Gain1 to Gain2 at time t_0



Headset short circuit protection

The headset drivers have a built-in short-circuit protection feature that is enabled by default. If a short is detected during operation an interrupt request is generated, 'IT_ShortHsL' or 'IT_ShortHsR' (*AudIntSource2* register); if 'EnShortPWD' = 1 (*ShortCirConf* register) the driver is automatically disabled. In order to re-enable the driver the 'EnHsL' and 'EnHsR' bits must be set to "0" and back to "1" again. The automatic shut down of the drivers can be disabled, 'EnShortPWD' = 0, allowing only an IRQ request. The short circuit protection can be disabled with the 'HsShortDis' bit (*ShortCirConf* register).

Headset power supply and low power mode

Headset drivers have a separate external power supply (VddHs) that must be less than or equal to the audio internal supply VddAD_DA. This external supply can also be switched off without any problem if the drivers have been disabled in advance. The PSR of VddHs makes it suitable for a direct connection to an SMPS. See *Figure 27* for an example of Headset driver supply connections.

A low-power mode is available on headset drivers, 'HsLowPow' and 'HsDACLowPow[1:0] bits (*AnaConf1* register) with little performance degradation at the analog output.

Headset output impedance in power down

When the headset drivers are disabled, by default their outputs are in high impedance and floating between VddHs and VssHs. In this condition it is possible to apply an external voltage source to HsR and HsL with the strict limitation that the voltage source must be within VddHs and VssHs limits. Through the 'HsPullDEn' bit (*ShortCirConf* register) HsL and HsR output can be pulled down to ground. The Negative Charge Pump can be enabled to extend the allowed voltage range below the ground level. This allows the share of the headset connector as line-in connector.

Negative Charge Pump (NCP)

A charge pump, enabled by the 'EnCphs" bit (*AnaConf5* register), generates the negative voltage for headset drivers. Two possible supply voltages are provided for this block. The first (**VinVcphs** ball) is directly connected to the battery (from 2.3 V to 4.8 V), the second

one (VsmpsVcphs ball) can be a fixed 1.8 V supply or, in case 1.8 V is not available, it can be connected together with VinVcphs ball.

The output voltage of the charge pump is -1.7 V typ when supplied by the VinVcphs ball, and -1.2 V typ. when supplied by the VsmpsVcphs ball.

Note: By setting the 'HsAutoEn' bit to "1" (*AnaConf5* register)*, Headset drivers instead to be enabled through 'EnHsL/R' bits are automatically enabled through 'EnCpHs' bit.*

Envelope detection

On the DAC path an envelope detection circuit controls the switching between the two NCP supplies. If a High Efficiency (like an SMPS, can be Vio18 if available) supply voltage (~1.75<=VHE<=VddAD_DA) is available in the platform it is possible to increase the overall system efficiency. Note that not all SMPS's are suitable for this use, as the NCP has an impulsive current usage that might affect the SMPS behavior. In the example in *Figure 27* VHE=1.8V.

Three registers ('EnvDetHThre[3:0]' bits and 'EnvDetLThre[3:0]' bits in *EnvCPConf* register, 'EnvDetTime[3:0]' bits in *SigEnvConf* register) control the threshold of the switching and the decay time of the detection. The switching from VsmpsVcphs (1.8V) to VinVcphs happens immediately after the input signal becomes bigger than the programmed threshold ('EnvDetHThre[3:0]' bits), while the switching from VinVcphs to VsmpsVcphs (1.8V) is controlled from 'EnvDetLThre[3:0]' bits for the threshold and also from 'EnvDetTime[3:0]' bits for the decay time, to avoid excess switching (*SigEnvConf* register).

The envelope detection circuit is enabled with bit 'EnvDetCpEn' (*SigEnvConf* register). When the envelope detection is disabled, it is possible to manually select the supply ball of the NCP with 'CpLVEn bit' (*SigEnvConf* register). See *Figure 27* for an example of Envelope detection behavior.

HF and Vib digital power outputs

High Efficiency Class-D drivers are present for the Handsfree function (HF) and Vibra Motor control (Vib). Hands-Free drivers are enabled through 'EnHfL/R' bits, Vibrator drivers through 'EnVib(i)' bits (*AnaConf4* register). Class D generators and dedicated digital path are enabled through 'EnDACHfL/R' and 'EnDACVib(i)' bits (*DAPathConf* register). To drive a lower speaker impedance, 4 Ω, it is possible to short-circuit both outputs through 'ParlHf' bit (*ClassDConf1* register), in this case HfL outputs are used.

In order to have maximum flexibility, the supply voltages of HF and Vib are independent and they can exceed or be below the battery voltage, so that the output power is not limited by battery discharge. The circuit that provides the supply voltage above the battery level is not provided inside AB8500 and it has to be selected considering the impulsive current request from the class-D drivers.

The HF and Vib paths have a + 9 dB gain on the DA path, that means that when a full scale digital sine wave signal is present on the DA path and the path gains are set to 0dB a +9dBV_{rms} nominal signal will be present at the output. Of course, if the supply voltage is not high enough, saturation will occur at the output.

The Vib outputs can also be controlled by control registers instead of DA paths (from *PWMGenConf1* to *PWMGenConf5* registers). Note that the PWM modulation duty cycle described in the control register does not directly correspond to the PWM modulation duty cycle at the Vib output. The reason for this is to guarantee that the output power is not dependent on the Vib supply voltage.

The Vib drivers can directly drive a 16 Ω vibra motor (with a minimum start up impedance of 10 Ω) or a high impedance capacitive piezo component.

The Vibra amplifier has a fixed +9 dB gain, while the PWM modulator from control register has a +7dB gain at 100% duty cycle, below is an example how to calculate the output level from the programmed PWM level.

– Example with duty cycle P=29%, N=71%:
  Vout=(0.29-0.71)*dB^{-1}(9+7)=-2.65$V_{AVG,}$ Where $dB^{-1}(n)=10^{(n/20)}$

  The (9+7) stands for: Path gain, PWM gain.

  The V_{AVG} unit means that a constant value is programmed in the PWM modulation control registers and a PWM signal is present at the Vibra output with an average voltage that corresponds to the programmed constant.

  Following is a list of PWM ideal output level versus programmed PWM level:

PWMP	PWMN	V_{AVG}
0%	100%	-6.32
29%	71%	-2.65
37%	63%	-1.64
50%	50%	0.00
63%	37%	1.64
71%	29%	2.65
100%	0%	6.32

Line out drivers

When stereo HF class-D drivers are not needed it is possible to use the same HF output pins to provide a stereo differential line-out signal. In order to avoid output driver conflict the line-out function can be enabled only if the HF enable bits, ‘EnHfL/R’ bits) are set to “0” (*AnaConf4*. register).

The two line-out paths can carry a stereo signal that comes from the 2 Hs DACs or a mono signal from the Ear DAC. The enable and path control of the line-out function is done through ‘EnLOL/R’ and ‘HsL/RDACToLOL/R’ bits (*AnaConf5* register).

The Line-out drivers can be muted by muting the corresponding DAC, ‘MutDACxx’ bits (*MuteConf* register)

3.6.12 Audio module supply options

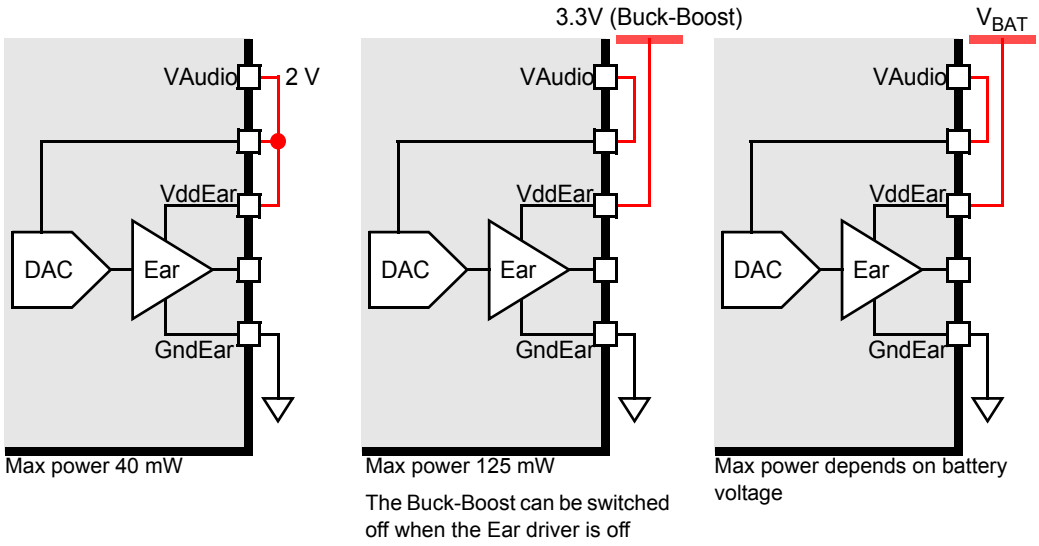
In this section several supply options are described, but as the Earpiece and headset pre-amplifier are supply through Vaudio LDO, this one must, for all the options, be enabled through the ‘VaudioEna’ bit (VaudioSupply register).

VddEar supply ball (*Figure 26*)

Depending of the output power required in the earpiece, VddEar ball can be connected either to Vaudio ball or to external supply, the maximum voltage of this output supply must be less than 4.8 V.
If the VddEar ball is connected to Vaudio ball, the earpiece driver (Earn, Earp) is able to deliver 40 mW in a 32-Ω earpiece transducer.

If the VddEar ball is connected to an external supply, the earpiece driver (Earn, Earp) is able to deliver 125 mW in a 32-Ω earpiece transducer, if the external supply has an output voltage between 3.2 and 4.8 V.

Figure 26. Ear output stage driver supply configurations

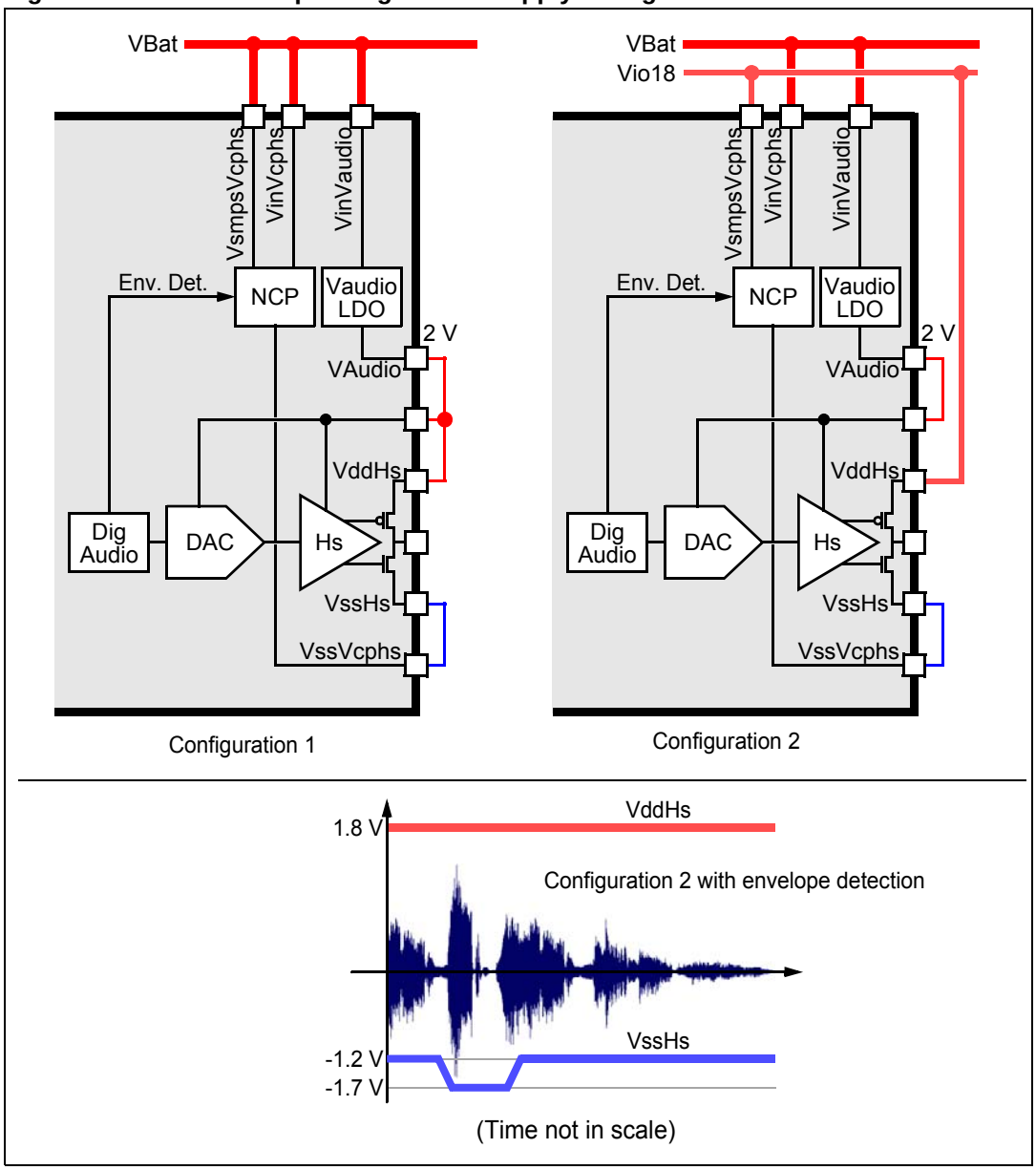


VddHs and SmpsVcphs balls

The stereo headset driver can be supplied in two ways (*Figure 27*):

- Configuration 1 (AB class Mode)
  - The VddHs ball is connected to Vaudio ball.
  - The SmpsVcphs ball is connected to Vbat supply.
  - Input of negative charge pump always connected to the VinVcphs ball.
- Configuration 2 (G class mode, lower power consumption)
  - The VddHs ball is connected to Vio18 supply
  - The SmpsVcphs ball is connected to Vio18 supply.
  - The digital audio subsystem detects the envelop of the audio signal and depending of its value connects the input supply of the negative charge pump to the VinVcphs ball or to the SmpsVcphs ball.

Figure 27. Headset output stage driver supply configurations



3.7 TVout module

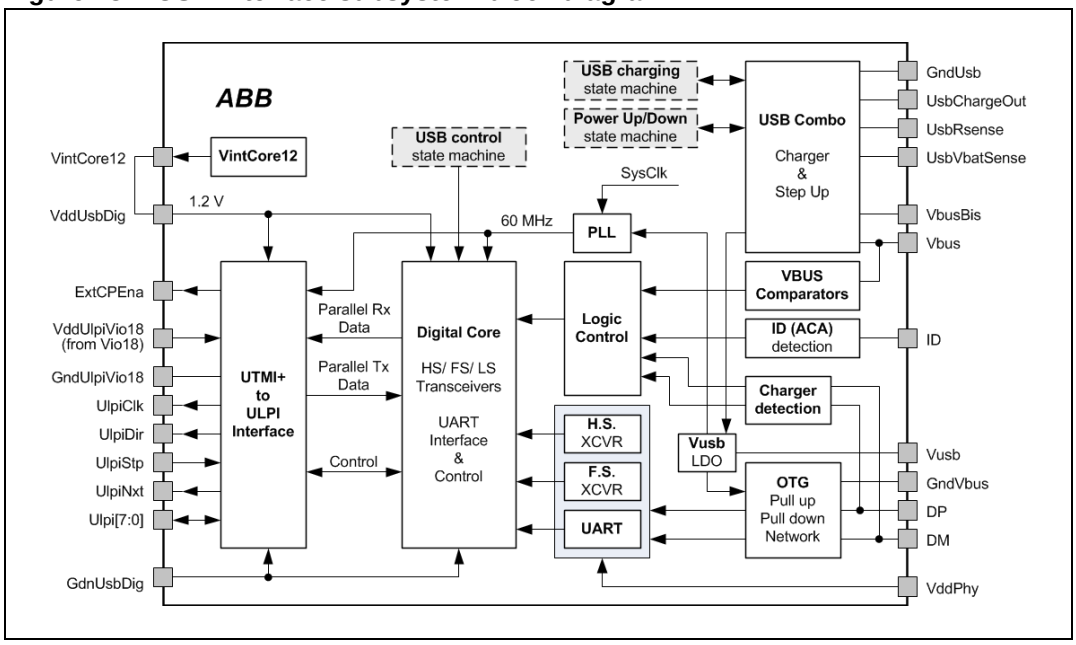
This information is not in public domain

3.8 USB 2.0 high speed OTG interface

3.8.1 Main Features

Figure 28 describes the USB Interface subsystem

Figure 28. USB interface subsystem block diagram



The USB interface subsystem supports the following features:

- USB 2.0 standard (LS, FS and HS)
- On-The-Go and Embedded Host supplement specification (v2.0)
  - Supports OTG Host, OTG peripheral functionality device and Embedded Host
  - Vbus output current of 250 mA with a DC-DC step up converter (50 mA for Vusb LDO, 200 mA for USB device)

Note: For Vbat > 3 V, current for USB device increases to 300 mA.

  - Supports SRP, HNP, Suspend/Resume/Remote wake up
  - Supports Attach Detection Protocol (ADP)
- Battery Charging Specification to USB standard v1.1
  - Implements Data connect and Charger detection
  - Required support of “Dead Battery Provision”
  - Supports Accessory Charger Adapter (ACA)
- Supports Link Power Management
- CARKIT standard
  - Supports UART mode

  - Does not support Audio CARKIT switches
- ULPI interface with USB link controller as described in specification v1.1 (8-bit SDR @1.8 V)
  - Supports 3-pin and 6-pin serial mode
- AB8500 wakes up from USB plug detection
- Implements choke and external component compensation

The USB subsystem supports three main operating modes:

- Active mode: full functionality
- Active sleep mode: USB link in suspend or asynchronous mode, wake up from Bus event or controller request USB link controller might be in deep sleep)
- Deep sleep mode: AB8500 in deep sleep, cable attachment triggers platform wake up and possibly charging detection

Note: The AB8500 USB subsystem can be disabled by grounding the Vbus ball and tying the ID ball to the battery supply at platform level. This will permanently disable USB charging, OTG supply generation and USB Phy.

3.8.2 Power consumption characteristics

This information is not available in the public domain.

3.8.3 USB application description

This information is not available in the public domain.

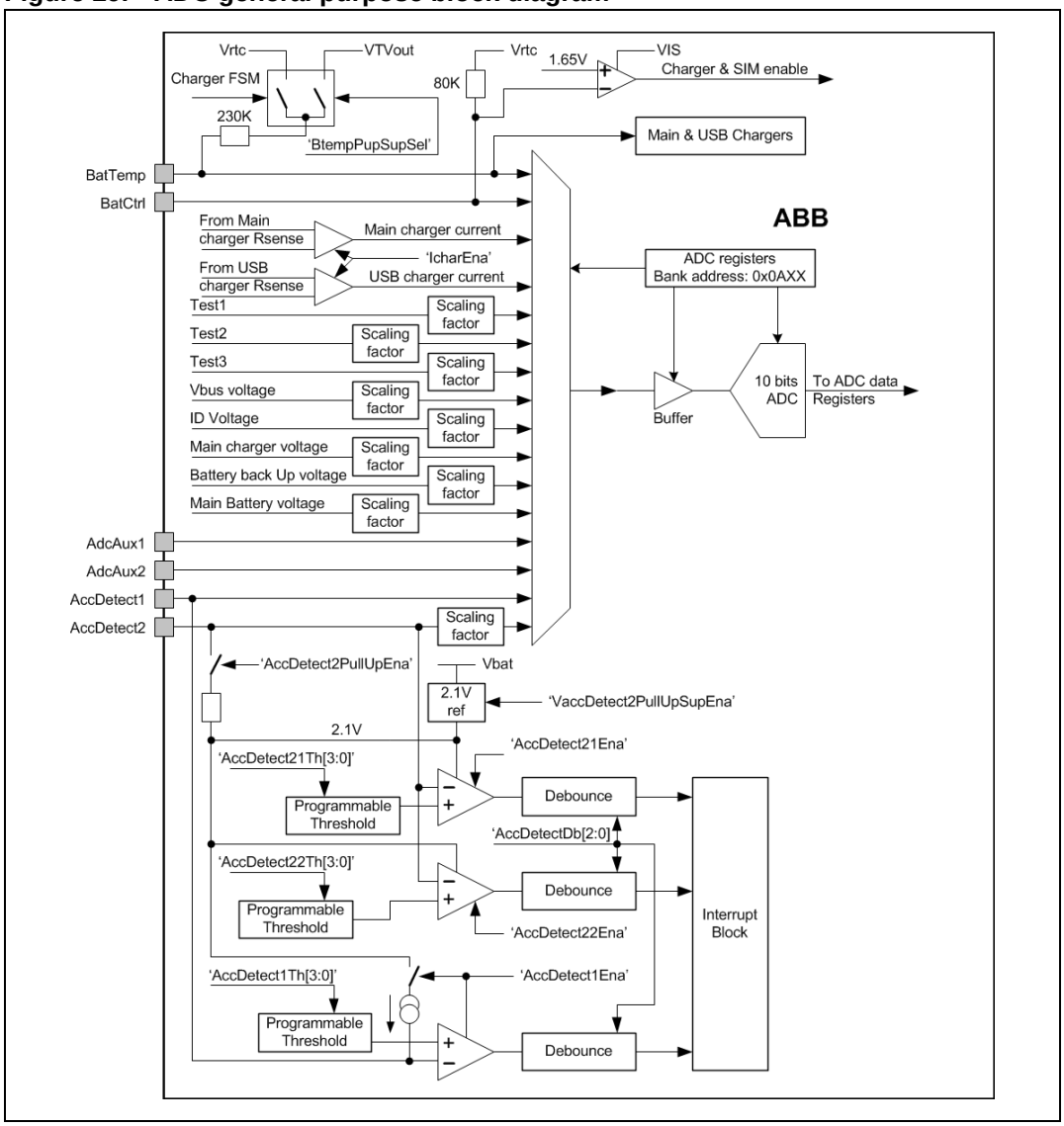
3.8.4 ULPI functional description

This information is not available in the public domain.

3.9 ADC general purpose

Figure *29* illustrates the ADC general purpose block diagram.

Figure 29. ADC general purpose block diagram



The ADC general purpose inputs are:

- External sources:
  - **AdcAux[2:1]**: Two auxiliary inputs used to measure the analog input voltage value. (for example: Phone temperature measurement through an external pull-up and an external NTC).
  - **AccDetect[2:1]**: Two accessory detection inputs used to detect the plug-in of an external accessory (for example: headset). The AccDetect1 input has a comparator, this is used to compare the analog input value to the internal threshold, its threshold is set though the 'AccDetect1Th[3:0] bits (*AccDetectDb1Th* register). The AccDetect2 input has two comparators, this is used to compare the analog input value to internal thresholds, its thresholds are set through the

'AccDetect2(i)Th[3:0] bits (*AccDetect2Th* register). These inputs are debounced inputs, the debounce time is set through the 'AccDetectDb[2:0] bits (*AccDetectDb1Th* register).
Before to starting a detection of an accessory, the feature must be configured through the *AccDetectCtrl* register.

* Depending which comparator is used by setting to "1" the corresponding 'AccDetect(i)Ena' bit.

* Depending on the accessory to be detected. An internal 2.1 V supply cannot be enabled through the 'VaccDetect2PullUpSupEna' bit

- For AccDetect1 a 2 µA current source is automatically enabled, previously done through the 'AccDetect1Ena' bit

- For the AccDetect2 comparators a pull up resistor can be connected through the 'AccDetect2PullUpEna' bit.

Each time an accessory detector output state changes, low to high or high to low, the associated interrupt 'IT_AccDetect(i)dBR' or 'IT_AccDetect(i)dBF' is generated, (*ITLatch5* register) these interrupts can be masked (*ITMask5* register).

  - **BatTemp**: Input dedicated to measure battery temperature through an external NTC. This ball is also directly connected to AB8500 charger modules and used to control the charger state machines. The 80 kΩ pull up resistor is controlled by the state machine and can also be controlled through the 'BtemPupSupSel' bit (*GPADCCtrl1* register).

- Internal sources:
  - Main battery voltage.
  - Battery backup voltage.
  - Vbus voltage
  - Main charger voltage
  - Main charger current
  - USB charger current
  - ID input voltage
  - Three inputs for test purposes.

The main characteristics of the ADC are:

- Supplied by VTVout LDO.
- Analog to digital conversion could be done without average or with a sampling average of 4, 8 or 16, Values to be confirmed).
- The sample conversion time is 2.6 µs.
- Max input voltage for ADC conversion: 1.35 V, input signals higher than this value are affected by a scaling factor.

ADC feature is enable by 'ADCEna' bit (*GPADCCtrl1* register)

By enabling the internal buffer, 'BufEna' bit = "1" (*GPADCCtrl1* register) the input capacitance is reduced, recommendation is to always enable this buffer, if 'BufEna' bit = "0", the buffer is bypassed. 'BufEna' bit must not change during conversion.

- Software control
  - The input source is selected through the 'ADCSwSel[4:0]' bits (*GPADCCtrl2* register)

  - The conversion can be averaged, the number of conversions, up to 16, to obtain the average value is programmed by ‘ADCSwAverage[1:0]’ bits (*GPADCCtrl2* register) and starts through the ‘ADCSwConvert’ bit (*GPADCCtrl1* register)
  - When ended the average value is stored in “GPADCSwData[9:0]’ bits (*GPADCSwDataL* and *GPADCSwDataH* registers), an interrupt is generated on IntDB8500n ball and the ‘GPSwADCConv’ bit is set to “1” (*ITSource5* register), this interrupt is latched in *ITLatch5* register and can be masked in *ITMask5* register.

- Hardware control, conversion is initiated by GPADCTrig ball (for example: can be used to test the battery voltage during a GSM burst if this information is sent on this ball by the RF sub-system)
  - The edge on which the conversion starts is selected through the ‘GPADCTrigEdge’ bit (*GPADCCtrl1* register)
  - The delay between the GPADCTrig ball edge and conversion start is set through the ‘GPADCTrigTimer[7:0]’ bits (*GPADCTrigTimer* register)
  - The input source is selected through the ‘ADCHwSel[4:0]’ bits (*GPADCCtrl3* register)
  - The conversion can be averaged, the number of conversions, up to 16, to obtain the average value is programmed by ‘ADCHwAverage[1:0]’ bits (*GPADCCtrl3* register) and starts through the ‘GPADCTrigEna’ bit (*GPADCCtrl1* register)
  - When ended the average value is stored in “GPADCHwData[9:0]’ bits (*GPADCHwDataL* and *GPADCHwDataH* registers), an interrupt is generated on **IntDB8500n** ball and ‘GPHwADCConvEnd’ bit is set to “1” (*ITSource5* register), this interrupt is latched in *ITLatch5* register and can be masked in *ITMask5* register.

Note: If both hardware and software conversion are enabled, if a software conversion starts and a hardware conversion is requested during the software conversion, priority is given to the hardware conversion, when hardware conversion is ended, software conversion is re-initialized and starts again automatically.

Table 10 describes AB8500 ball voltage input range and the LSB of each input channel.

Table 10. ADC Input channel information

‘AdcSwSel[4:0]’ ‘AdcHwSel[4:0]’	Balls or internal measurement	AB8500 ball range	AB8500 LSB
00001	BatCtrl ball	0 to 1.35 V	1.32 mV
00100	AccDetect1 ball		
00110	AdcAux1 ball		
00111	AdcAux2 ball		
01101	Reserved		
00010	BatTemp ball	0 to 1.35 V (100°C)	1.32 mV (~0.1°C)
00011	Main charger voltage	0 to 20.03 V	19.56 mV
01001	Vbus voltage		
00101	AccDetect2 ball	0 to 2.5 V	2.44 mV
01110	ID detection	0 to 1.35 V	1.32 mV

Table 10. ADC Input channel information

'AdcSwSel[4:0]' 'AdcHwSel[4:0]'	Balls or internal measurement	AB8500 ball range	AB8500 LSB
01000	Battery voltage	2.3 to 4.8 V	2.44 mV
01010	Main charger current(1)	0 to 1.5 A	1.46 mA
01011	USB charger current(1)		
01100	BackUp battery	0 to 3.2 V	3.13 mV
01111	Test 1	0 to 4.8 V	4.69 mV
10000	Test 2		
10001	Test 3		

1. To do a current measurement 'IcharEna' bit (*GPADCCtrl1* register) must be set to "1".

ADC calibration

Three ADC inputs are calibrated, Main Charger voltage (vmain), BatTemp (btemp) and Battery voltage (vbat).

For each input a minimum (low) and a maximum (high) input voltage are injected and stored in an internal memory, this information can be retrieved by the host at the register addresses given in *Table 11*.

In *Table 11* the ideal values are given, with the ideal values and the values stored at the register address given in *Table 11*, the host can calibrate the ADC.

Table 11. ADC calibration

Register	Address Ideal value	Data (bits)							
		7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
GpADCCal1	0x150F	Reserved						vmain_high9	vmain_high8
	ideal value	N/A						**1**	**1**
GpADCCal2	0x1510	Reserved		vmain_high7	vmain_high6	vmain_high5	vmain_high4	vmain_high3	vmain_high2
	ideal value	N/A		**1**	**1**	**1**	**0**	**0**	**1**
GpADCCal3	0x1511	vmain_high1	vmain_high0	vmain_low4	vmain_low3	vmain_low2	vmain_low1	vmain_low0	btemp_high9
	ideal value	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**
GpADCCal4	0x1512	btemp_high8	btemp_high7	btemp_high6	btemp_high5	btemp_high4	btemp_high3	btemp_high2	btemp_high1
	ideal value	**1**	**1**	**1**	**0**	**1**	**1**	**0**	**0**
GpADCCal5	0x1513	btemp_high0	btemp_low4	btemp_low3	btemp_low2	btemp_low1	btemp_low0	vbat_high9	vbat_high8
	ideal value	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
GpADCCal6	0x1514	vbat_high7	vbat_high6	vbat_high5	vbat_high4	vbat_high3	vbat_high2	vbat_high1	vbat_high0
	ideal value	**1**	**1**	**0**	**1**	**0**	**1**	**1**	**0**
GpADCCal7	0x1515	vbat_low5	vbat_low4	vbat_low3	vbat_low2	vbat_low1	vbat_low0	Reserved	
	ideal value	**1**	**0**	**0**	**0**	**0**	**1**	N/A	

- Ideal values, output ADC codes, in decimal, corresponding to injected input voltages during manufacturing are as follows:
  - vmain_high[9:0]: Vin = 19.5 V / Code_ideal: 997
  - vmain_low[4:0]: Vin = 0.315 V / Code_ideal: 16
  - btemp_high[9:0]: Vin = 1.3 V / Code_ideal: 985
  - btemp_low[4:0]: Vin = 21 mV / Code_ideal: 16
  - vbat_high[9:0]: Vin = 4.7 V / Code_ideal: 982
  - vbat_low[5:0]: Vin = 2.38 V / Code_ideal: 33

3.10 SIM card interface

This information is not available in the public domain.

3.11 PWM generator

The AB8500 has three PWM generators, PWM generators are programmed by PWM registers (See *Section 4.4.14: PWMOut generators*), the parameters are:

- Enabling, ‘EnaPWMOut(i)’ bits
- Frequency, ‘FreqPWMOut(i)[3:0]’ bits: 293 to 551 Hz
- Duty cycle, ‘DutyPWMOut(i)[9:0]’ bits: 1/1024 to 100% with a 1/1024 step

PWM generator input clock is SysClk or UlpClk.

3.12 RTC and backup battery management

3.12.1 Backup battery charger

Backup battery charger control

(see *Figure 30*)

Output current and voltage of the backup battery charger are programmable through the *RtcBackupChg* register. Backup current source charger is enabled in Operating mode when:

- OTP is downloaded
- ‘BupchEna’ bit (*RtcCtrl* register) is high, which enables the charger (disabled by default, reset by PORnVrtc)
- Battery voltage is above backup battery voltage.
- Backup battery voltage is below programmed backup battery threshold.

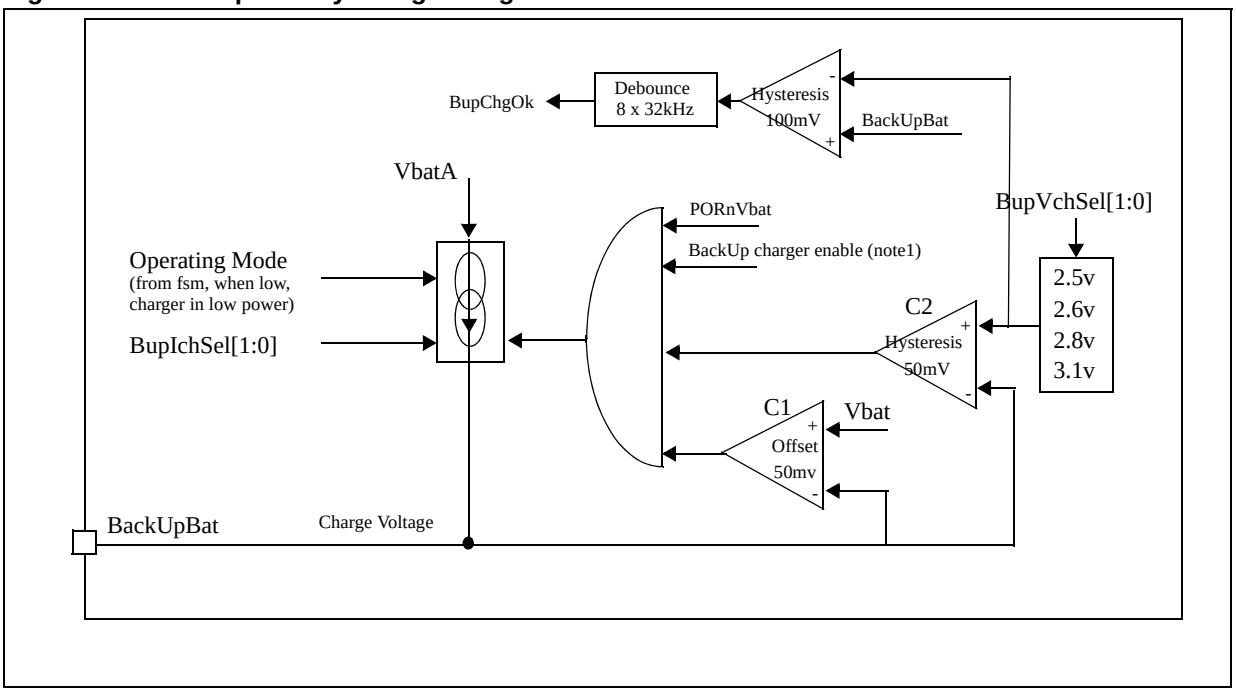
When the AB8500 is in Off mode, the ‘BupChOffValid’ bit (*RtcCtrl* register) keeps the backup battery charger enabled in a low power mode:

- If ‘BupChOffValid’ bit is low: backUp charger is enabled when ‘BupChEna’ bit is high and AB8500 is in Operating mode, its current value is set through the ‘BupIchSel[1:0] bits (*RtcBackupChg* register) and it charging voltage through the ‘BupVchSel[1:0] bits.
- If ‘BupChOffValid’ bit is high: backUp charger is enabled when ‘BupChEna’ bit is high and AB8500 Operating mode controls backup charger low power mode.

For an application without a backup battery BackUpBat ball should be tied to Vbat. The Backup charger should be disabled to avoid consumption.

When the backup charger is off and Vbat is below the backup voltage or main battery disconnected, then there is no leakage from BackUpBat to Vbat (max 0.1 µA).

Figure 30. Backup battery charger diagram



Note: See comments above on BackUp battery charger enable conditions.

Table 12. Back Up charger state truth table

'BupChEna' & Vbat > BackUp & BackUp < 'BupVchSel[1:0]'	fsm state	'BupChOffValid'	Back Up charger state
0	x	x	**Disable**
1	PwrOff	0	**Disable**
1	PwrOff	1	**Enable in Low Power**
1	PwrOn	x	**Enable in HP**

When the BackUp battery voltage reaches the programmed voltage, 'IT_BupChgOk' bit is set to "1", if it goes below the programmed voltage minus the hysteresis, 'IT_BupChgNok' bit is set to "1" (*ITLatch5* register), these interrupts can be masked (*ITMask4* register).

3.12.2 RTC supply management

The Vrtc LDO supplies RTC Xtal oscillator, counters and registers which are reset by the PORnVrtc cell (Power-on Reset supplied by Vrtc).

Note: The 32 kHz oscillator embedded two 20 pF capacitors, one on each ball, XtalIn32kHz and XtalOut32kHz, so no external capacitors are required in these balls.

Vrtc LDO is supplied by:

- Either VIS which corresponds to Vbat or charger regulated voltage
- Or backup battery

If PORnVrtc internal signal is high, Vrtc will be supplied in the following priority order:

- Battery (if PORnVbat is high)
- Main charger (if PORnVbat is low, main charger plug detected)
- Vbus (if PORnVbat is low, Vbus detected)
- Backup battery (if PORnVbat is low).

Bit ‘ForceBackUp’ (*RtcForceBackup* register) forces the **BackUp** ball to supply RTC.

Table 13. Vrtc generation truth table

PORnVrtc	‘ForceBackUp’	PORnVIS	Vrtc generation
0	0	0	Hiz
1	0	0	VbackUp
0	1	0	Hiz
1	1	0	VbackUp
0	0	1	VIS
1	0	1	VIS
0	1	1	VIS
1	1	1	VbackUp

3.12.3 RTC Xtal and counters

(see *Figure 31*)

RTC bloc

Watchtime registers make it possible to program:

- RTC 21 bits counter. 16 bits (connected to MSB counter bits) corresponds to an accuracy less than 1 ms and a range of 60 s. (WatchTimeSec[15:0] bits)

- RTC 24 bits counter: corresponds to an accuracy of 60 s and a range up to 31 years. (WatchTimeMin[23:0] bits)

RTC watchtime deviation is corrected by the *RtcCalibration* register every 60 s. *RtcCalibration* register is 7 bits + sign register, is supplied by Vrtc, and is at 0 by default.

The correction accuracy is 30.5 µs which corresponds to 0.5 ppm of the 32 kHz clock. The correction range is 3.875 ms which corresponds to +/- 65 ppm of the 32 kHz clock.

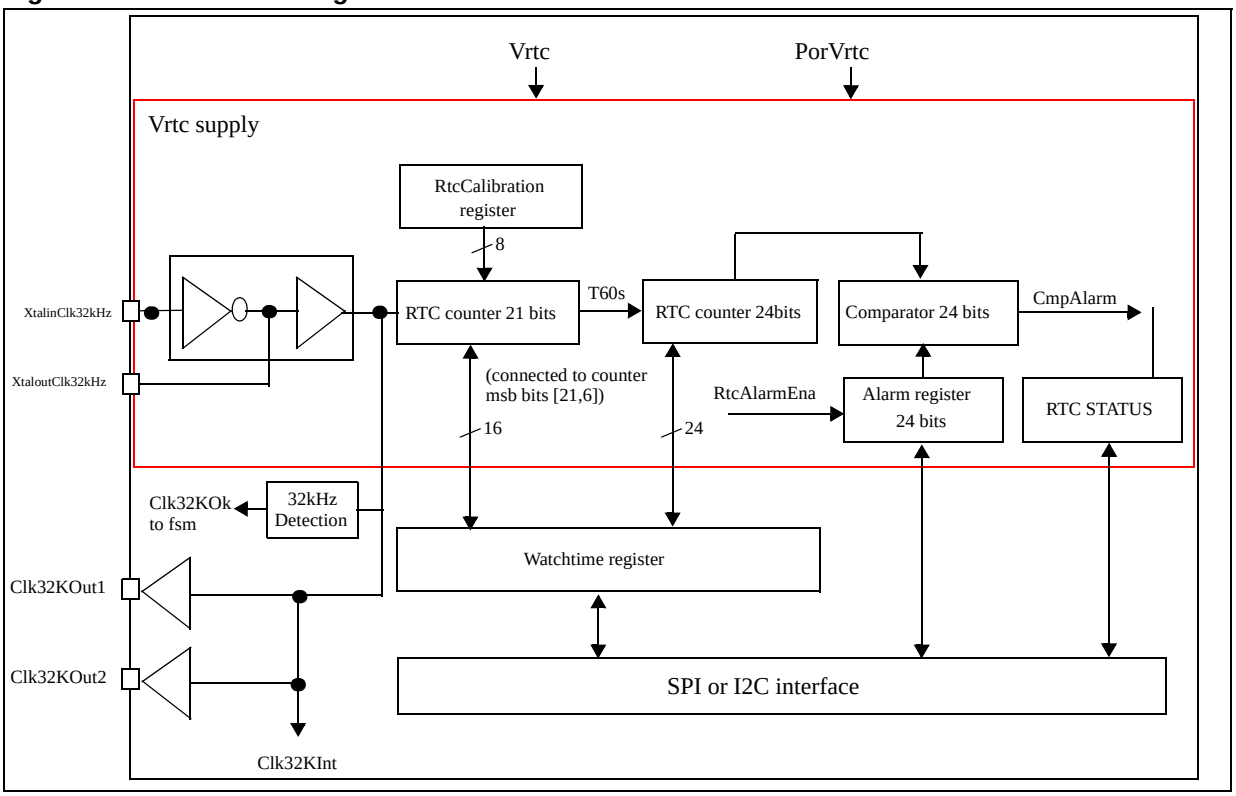
Each 60 s an interrupt is generated, ‘IT_Rtc60s’ bit asserted (*ITLatch3* register), this interrupt can be masked (*ITMask3* register).

Alarm registers on 24 bits make it possible to program the RTC alarm.

Clk32KOut1/2 balls are enabled in operating mode.

Clk32KOut2 output can be disabled using ‘Clk32kOut2Dis’ bit (STw4500Ctrl3 register).

Figure 31. RTC block diagram



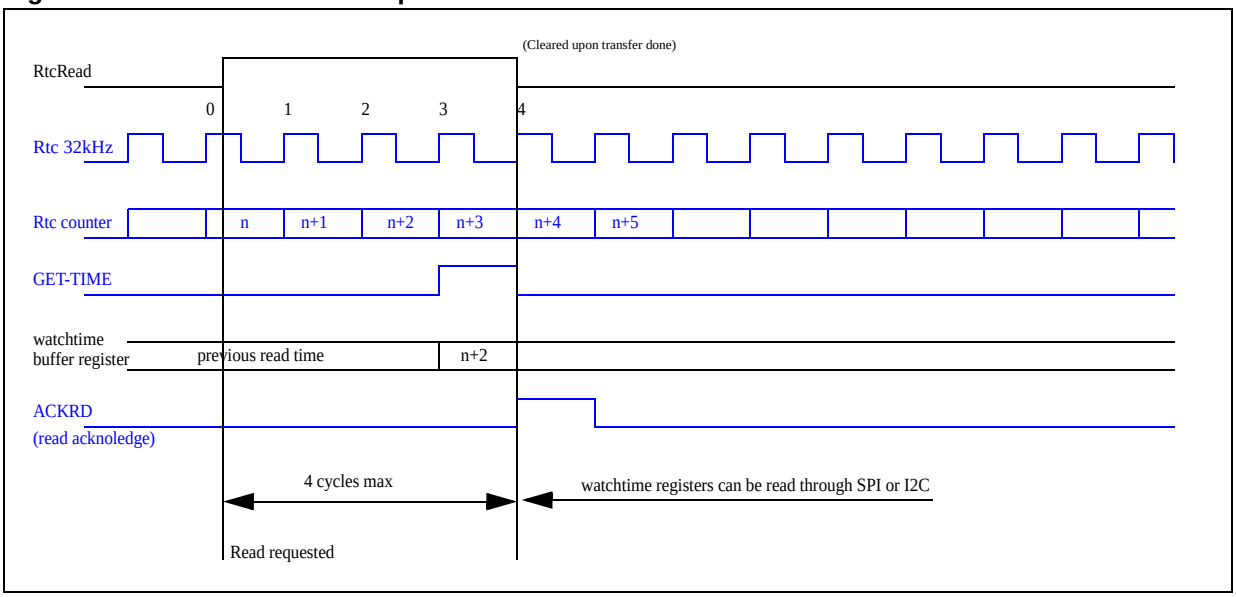
Reading watchtime registers

(See *Figure 32*)

Due to the asynchronous clock between “SPI or I^2C interface” and the “32 kHz”, at first the APE should set the high bit ‘RtcRead’ (*RTCReadRequest* register). When counter data is stable:

- Data is transferred in watchtime buffer register.
- ‘RtcRead’ bit is cleared.
- APE should wait 4 x 32 kHz cycles.
- APE can read watchtime registers.

Figure 32. Rtc counter read operation



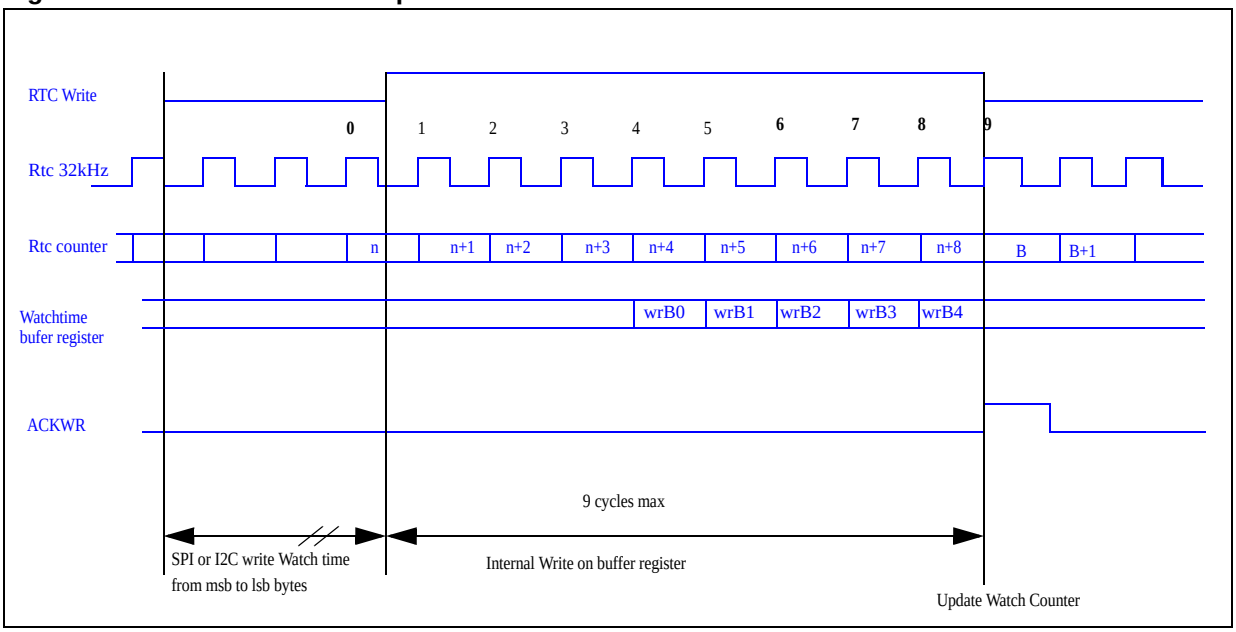
Write watchtime registers

(See *Figure 33*)

To write data into the RTC counter:

- write to *Watchtime registers* in the following order:
  - WatchtimeMinHigh
  - WatchtimeMinMid
  - WatchtimeMinLow
  - WatchtimeSecHigh and then
  - WatchtimeSecMid
- Data is transferred from Watchtime registers to the RTC counter when the register writing sequence is detected.
- APE should wait for 9 x 32 kHz cycles before writing again in watchtime register.

Figure 33. Rtc counter write operation



RTC alarm

RtcAlarm allows to the AB8500 to be turned on. In both modes, the RtcAlarm sends an interrupt through the IntDB8500n ball. This interrupt is stored in the *ITLatch3* register and can be masked in the *ITMask3* register.

RtcAlarm is enabled by the ‘RtcAlarmEna’ bit of the *RtcCtrl* register. Alarm data is set by the Alarm register. (20 bits correspond to more than 1 year).

‘RTCAlarm’ wake up information is stored in the TurnOnstatus register.

3.12.4 RTC status

The ‘RtcStatusData’ bit of the *RtcCtrl* register is cleared only by PorRtc. It can be used to indicate that the Vrtc supply has failed.

A delay of 4 x 32 kHz clock cycles must be awaited between two write accesses in *RtcCtrl* register.

The status of the 32 kHz clock used, from internal RC or from crystal, is stored in *RtcSwitchStatus* register.

3.13 Miscellaneous

3.13.1 GPIO

The GPIOs alternate functions are described in *Table 14*. The alternate ball configurations are defined through the *GpioSel1* up to the *GpioSel6* registers and by the *AlternatFunction* register.

Then used as GPIO they are configured through the following:

- *GpioDir1* up to *GpioDir6* registers for direction (input/output)
- *GpioPud1* up to *GpioPud6* registers for pull up / pull down, when configured as input
- *GpioOut1* up to *GpioOut6* registers for Low/high when configured as output

16 GPIOs have interrupt capability, interruptions are generated in the *ITSource7* and *ITSource8* registers, are latched in the *ITLatch7* up to *ITLatch10* registers and can be masked in the *ITMask7* up to *ITMask10* registers.

Table 14. Balls with alternate function

Ball					Ball			
Default	**Alternate function**			**Interrupt capability**	**Default**	**Alternate function**		**Interrupt capability**
SysClkReq2	GPIO1			No	UsbUiccData	GPIO22		No
SysClkReq3	GPIO2			No	UsbUiccSe0	GPIO23		No
SysClkReq4	GPIO3			No	SysClkReq7	GPIO24		Yes
SysClkReq6	GPIO4			No	SysClkReq8	GPIO25		Yes
YCbCr0	GPIO6			Yes	GPIO26			No
YCbCr1	GPIO7			Yes	Dmic12Clk	GPIO27		No
YCbCr2	GPIO8			Yes	Dmic12Dat	GPIO28		No
YCbCr3	GPIO9			Yes	Dmic34Clk	GPIO29		No
GPIO10	YCbCr4	HiqClkEna		Yes	Dmic34Dat	GPIO30		No
GPIO11	YCbCr5	UsbUiccPd		Yes	Dmic56Clk	GPIO31		No
GPIO12	YCbCr6	I2CTrig1		Yes	Dmic56Dat	GPIO32		No
GPIO13	YCbCr7	I2CTrig2	UsbVdat	Yes	ExtCPEna	GPIO34		No
PWMOut1	GPIO14			No	GPIO35			No
PWMOut2	GPIO15			No	ApeSpiClk	GPIO36		Yes
PWMOut3	GPIO16			No	ApeSpiCSn	GPIO37		Yes
AD_Data1	GPIO17			No	ApeSpiDout	GPIO38		Yes
DA_Data1	GPIO18			No	ApeSpiDin	GPIO39		Yes
Fsync1	GPIO19			No	ModSCL	GPIO40		Yes
BitClk1	GPIO20			No	ModSDA	GPIO41		Yes
UsbUiccDir	GPIO21			No	SysClkReq5	GPIO42		No

3.13.2 Thermal shutdown

The thermal sensor cell contains two thresholds:

- Thermal warning threshold at 130°C which generates an interrupt, ‘IT_TempWarm’ bit (*ITLatch1* register).
- Thermal shutdown threshold at 150°C causes turnoff of the AB8500.

Table 15. Thermal thresholds

Threshold	Min	Typ	Max	Unit
Thermal warning rising threshold	118	130	142	°C
Thermal warning falling threshold	88	100	112	°C
Thermal shutdown rising threshold	138	150	162	°C
Thermal shutdown falling threshold	108	120	132	°C

It is not recommended to do it, but it is possible to disable the thermal shutdown feature through the ‘ThsdEna’ bit (STw4500Ctrl3 register).

3.13.3 OTP management

This information is not available in the public domain.

4 Registers

4.1 Register format

SPI link

13-bit address format / 8-bit data format

Table 16. Register address format(1)

Clk16	Clk15	Clk14	Clk13	Clk12	Clk11	Clk10	Clk9	Clk8	Clk7	Clk6	Clk5	Clk4	Clk3	Clk2	Clk1
R/W	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	-	-

1. Bx corresponds to Bank number X, Ay corresponds to address number Y

PRCMU I2C

Table 17. Register address format

b7	b6	b5	b4	b3	b2	b1	b0
AdrID6	AdrID5	AdrID4	AdrID3	AdrID2	AdrID1	AdrID0	R/$\overline{W}$
0	1	Bank register address					R/$\overline{W}$
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
RegADR7	RegADR6	RegADR5	RegADR4	RegADR3	RegADR2	RegADR1	RegADR0
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Modem I2C

Table 18. Register address format

b7	b6	b5	b4	b3	b2	b1	b0
AdrID6	AdrID5	AdrID4	AdrID3	AdrID2	AdrID1	AdrID0	R/$\overline{W}$
1	0	Bank register address					R/$\overline{W}$
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
RegADR7	RegADR6	RegADR5	RegADR4	RegADR3	RegADR2	RegADR1	RegADR0
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

4.2 Register reset sources

*Note: For each register, the "**Reset:>"** location indicates which signals reset the register.*

There are four internal reset signals for registers: DigPORn, SwitchOffRstn and StdRegRstn, PORnVrtc.

- DigPORn: VIS is not present, no charger connected or Vbattery supply detected.
- SwitchOffRstn: one of the Switch Off event appends:
  - ON/OFF key press duration (**PonKey1** ball) is controlled by a 10-s max, programmable timer; if the key press duration is longer than the value programmed in the timer, AB8500 goes back to OFF mode.
  - "SWOff" bit or 'ThDB8500SwOff' bit of STw4500Ctrl1 register is set high.
  - Internal watchdog timer expires, its value is programmed between 1 and 128 s in MainWDogTimer register and its default value is 32 s.
  - Battery goes below BattOK threshold; this threshold is programmable by OTP. If charger is still present, AB8500 is turned ON again as soon as battery rises above BattOK threshold,
  - Thermal shutdown protection occurs.
  - Battery removal.
  - 32 kHz oscillator stops running
- StdRegRstn: one of the reset condition appends
  - **ResetAB8500n** ball goes to low level
  - 'SwReset4500n' bit = "0" (STw4500Ctrl1 register)

    The reset source is stored in Resetstatus register
- PORnVrtc, **Vrtc** ball supply goes below 1.5 V

*Note: Through the STw4500Ctrl2 register bits, it is possible for **ExtSupply(i)Ena** balls, Vsmps1, Vmod, Vaux1, Vaux2 and Vaux3 to not validate their reset so as to keep the previous programmed values. (for example if Vaux1 was set ON, in HP mode and with a defined output voltage it will stay in this configuration).*

4.3 Register access

Registers can be accessible through Ape I2C (PRCMU I2C) or Modem I2C or SPI. Different configurations can be programmed by 'SerialCtrl[3:0]' bits of ReguSerialCtrl1 register.

Warning: The ReguSerialCtrl1 register is only accessible through PRCMU I2C. ReguSerialCtrl1 register is reset only by DigPORn and SwitchOffRstn.
Writing or reading to ReguSerialCtrl1 register allows the I^2C modem interface to be reset (if the I^2C modem is in wrong state, one way to reset it can be to write to ReguSerialCtrl1 register).

4.4 Register description

4.4.1 System control

This information is not available in the public domain.

4.4.2 Supply control

This information is not available in the public domain.

4.4.3 SIM control

This information is not available in the public domain.

4.4.4 USB registers

USB Control: Bank 0x5, Adr 10xxxxxx

UsbLineStatus — USB Line Status

7	6	5	4	3	2	1	0
UartMode	UsbLinkStatus[3:0]				VdatDet	VDMDet	VDPDet
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0580

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: USB charger management status.

[7]	**UartMode** 0: UART mode is not active 1: UART mode is active
[6:3]	**UsbLinkStatus[3:0]** 0000: Not configured 0001: Standard Host, not charging 0010: Standard Host, charging, not suspended 0011: Standard Host, charging, suspended 0100: Host charger, normal mode 0101: Host charger, HS mode 0110: Host charger, HS Chirp mode 0111: Dedicated USx charger 1000: ACA RID_A configuration 1001: ACA RID_B configuration 1010: ACA RID_C configuration, normal mode 1011: ACA RID_C configuration, HS mode 1100: ACA RID_C configuration, HS Chirp mode 1101: Host mode (IDGND) 1110: Reserved 1111: USB link not valid
[2]	**VdatDet** 0: No Host charger detected 1: Host Charger detected
[1]	**VDMDet** 0: DM Single Ended Receiver output is low 1: DM Single Ended Receiver output is high
[0]	**VDPDet** 0: DP Single Ended Receiver output is low 1: DP Single Ended Receiver output is high

UsbLineCtrl1 UsbLineCtrl1

7	6	5	4	3	2	1	0
Reserved	DMPU	DPPD	DMDP	DPPU	PhyResetn	UsbSwitchCtrl	IdDetADCEna
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0581

Type: R/W

Reset: 0x06 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: USB phy management.

[7]	Reserved
[6]	**DMPU** if 'UsbSwitchCtrl' = 0 0: DM Pull-Up disable 1: DM Pull-Up enable
[5]	**DPPD** if 'UsbSwitchCtrl' = 0 0: DP Pull-Down disable 1: DP Pull-Down enable
[4]	**DMPD** if 'UsbSwitchCtrl' = 0 0: DM Pull-Down disable 1: DM Pull-Down enable
[3]	**DPPU** if 'UsbSwitchCtrl' = 0 0: DP Pull-Up disable 1: DP Pull-Up enable
[2]	**PhyResetn** 0: PHY is reset (active low) 1: PHY is not reset
[1]	**UsbSwitchCtrl** Note: Functionality is controlled either by charger FSM or by this bit. Reading read MUX output; writing select bit, reset select charger FSM. 0: Pull-up and Pull-down switches (including ENC switches) are controlled by SPI or I^2C register 1: Pull-up and Pull-down switches (including ENC switches) are controlled by ULPI register (exclusive control)
[0]	**IdDetADCEna** 0: Disable ID detection through ADC 1: Enable ID detection through ADC

UsbLineCtrl2 UsbLineCtrl2

7	6	5	4	3	2	1	0
DMDP19Ena	ChargerMuxCtrl	UartLPModeEna	GateSysUlpClkToSmpsPwmSwat	Reserved			UsbChargDetEna
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0582

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: USB phy management.

[7]	**DMPD19Ena** Note: Functionality is controlled either by charger FSM or by this bit. Reading read MUX output; writing select bit, reset select charger FSM. 0: Disable DM 19.25 kΩ pull-down 1: Enable DM 19.25 kΩ pull-down Active only when 'ChargerMuxCtrl' = '1'
[6]	**ChargerMuxCtrl** 0: DM 19.25 kΩ pull-down and Single Ended Receiver controlled by ULPI 1: DM 19.25 kΩ pull-down and Single Ended Receiver controlled by SPI or I^2C for charger detection
[5]	**UartLPModeEna** 0: UART low power mode is not enabled 1: UART low power mode is enabled
[4]	**GateSysUlpClkToSmpsPwmSwat** 0: Clock not gated 1: Clock gated, sent only to audio digital
[3:1]	Reserved
[0]	**UsbChargDetEna** Note: this feature is automatically enabled when an USB cable is plugged 0: Disable USB charger detection 1: Enable USB charger detection

UsbLineCtrl3 UsbLineCtrl3

7	6	5	4	3	2	1	0
DCDCompEna	DatSrcEna	SDM_SNK	SDP_SNK	SDM_SRC	SDP_SRC	VdatSrcEna	IdatSnkEna
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0583

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: USB phy management.

[7]	**DCDCompEna (Data Connect Detection Enable)** Note: Functionality is controlled either by charger FSM or by this bit. Reading read mux output; writing select bit, reset select charger FSM. 0: Data Connect Detection is disabled 1: Data Connect Detection is enabled
[6]	**DatSrcEna (Data Connect 10 µA source Enable)** Note: Functionality is controlled either by charger FSM or by this bit. Reading read mux output; writing select bit, reset select charger FSM. 0: Data Connect source is disabled 1: Data Connect source is enabled
[5]	**SDM_SNK** Note: Functionality is controlled either by charger FSM or by this bit. Reading read mux output; writing select bit, reset select charger FSM. 0: SDM_SNK USB switch is opened 1: SDM_SNK USB switch is closed
[4]	**SDP_SNK** 0: SDP_SNK USB switch is opened 1: SDP_SNK USB switch is closed
[3]	**SDM_SRC** 0: SDM_SRC USB switch is opened 1: SDM_SRC USB switch is closed

[2]	**SDP_SRC** Note: Functionality is controlled either by charger FSM or by this bit. Reading read mux output; writing select bit, reset select charger FSM. 0: SDP_SRC USB switch is opened 1: SDP_SRC USB switch is closed
[1]	**VdatSrcEna** Note: Functionality is controlled either by charger FSM or by this bit. Reading read mux output; writing select bit, reset select charger FSM. 0: USB VDAT SRC comparator, VDAT DET comparator, VDAT_REF reference are disabled 1: USB VDAT SRC comparator, VDAT DET comparator, VDAT_REF reference comparators are enabled
[0]	**IdatSnkEna** Note: Functionality is controlled either by charger FSM or by this bit. Reading read mux output; writing select bit, reset select charger FSM. 0: USB IDAT SIN current source, VDAT DET comparator, VDAT_REF reference are disabled 1: USB IDAT SIN current source, VDAT DET comparator, VDAT_REF reference are enabled

UsbOTGCtrl — Usb OTG Control

7	6	5	4	3	2	1	0
Reserved		VbusValidEna	Reserved			IDHostEna	IDDevEna
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0587

Type: R/W

Reset: 0x0'OTP' (StdRegRstn, DigPORn, SwitchOffRstn)

Description: USB OTG.management

[7:6]	Reserved
[5]	**VbusValidEna** Note: Functionality is controlled either by charger FSM or by this bit. Reading read mux output; writing select bit, reset select charger FSM. 0: Disable VBUS Valid comparator 1: Enable VBUS Valid comparator
[4:2]	Reserved
[1]	**IDHostEna** Note: Functionality is controlled either by charger FSM or by this bit. Reading read mux output; writing select bit, reset select charger FSM. Default value can be fixed by 'OTP_IDDetectTurnOn' bit 0: Disable ID Host detection 1: Enable ID Host detection
[0]	**IDDevEna** Note: Functionality is controlled either by charger FSM or by this bit. Reading read mux output; writing select bit, reset select charger FSM. 0: Disable ID device detection 1: Enable ID device detection

UsbOTGStatus UsbOTGStatus

7	6	5	4	3	2	1	0
Reserved		DrvVbus	IDDetR4	IDDetR3	IDDetR2	IDDetR1	IDWakeup
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0588

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: ID resistance value management

[7:6]	Reserved
[5]	**DrvVbus** 0: 5 V generation is disabled 1: 5 V generation is enabled
[4]	**IIDDetR4** 0: ID resistance is below R4 1: ID resistance is above R4
[3]	**IDDetR3** 0: ID resistance is below R3 1: ID resistance is above R3
[2]	**IIDDetR2** 0: ID resistance is below R2 1: ID resistance is above R2
[1]	**IIDDetR1** 0: ID resistance is below R1 1: ID resistance is above R1
[0]	**IDWakeup** 0: ID resistance is floating (no micro-A plug detected) 1: ID resistance is grounded (micro-A plug detected)

UsbPHYStatus UsbPHYStatus

7	6	5	4	3	2	1	0
Reserved					HsMode	ChirpMode	SuspendModen
R	R	R	R	R	R	R	R

Address: BaseAddress+ 0x0589

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: USB Phy status

[7:3]	Reserved
[2]	**HsMode** 0: PHY is not in HS mode 1: PHY is in HS mode
[1]	**ChirpMode** 0: PHY is not in Chirp mode 1: PHY is in Chirp mode
[0]	**SuspendModen** 0: PHY is in Suspend mode 1: PHY is not in Suspend mode

UsbPhyCtrl UsbPhyctrl

7	6	5	4	3	2	1	0
Reserved						UsbDevice ModeEna	UsbHost ModeEna
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x058A

Type: R/W

Reset: 0x0X (StdRegRstn, DigPORn, SwitchOffRstn)

Description: USB phy control

[7:2]	Reserved
[1]	**UsbDeviceModeEna** Note: default value depends on charger Finite State Machine (FSM): when the AB8500 is in ON state, if PHY has been enabled by hardware in device mode then default value is 1 otherwise it is 0 0: Does not turn on USB PHY 1: Turn on USB PHY in Device mode (turn on sequence of USB PHY with no Vbus generation)
[0]	**UsbHostModeEna** Note: default value depends on charger FSM: when AB8500 is in ON state, if PHY has been enabled by HW in Host mode then default value is 1 otherwise it is 0) 0: Does not turn on USB PHY 1: Turn on USB PHY in host mode

UsbAdpProbeTimeCurrentL — Adp control

7	6	5	4	3	2	1	0
UsbAdpProbeTimeCurrent[7:0]							
R	R	R	R	R	R	R	R/W

Address: BaseAddress: 0x0591

Type: R

Reset: 0x00 (DigPORn)

Description: ADP current probe timer

[7:0]	**UsbAdpProbeTimeCurrent[7:0]** Time between two thresholds: UsbAdpTimeCurrent[10:0] x Clk32kHz period (max about 63.9 ms)

UsbAdpProbeTimeCurrentH — Adp Control

7	6	5	4	3	2	1	0
Reserved					UsbAdpProbeTimeCurrent[10:8]		
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0592

Type: R

Reset: 0x00 (DigPORn)

Description: ADP current probe timer

[7:3]	Reserved
[2:0]	**UsbAdpProbeTimeCurrent[10:8]** Time between two thresholds: UsbAdpTimeCurrent[10:0] x Clk32kHz period (max about 63.9 ms)

UsbAdpCtrl — Adp Control

7	6	5	4	3	2	1	0
Reserved				UsbAdpProbeTimeTh[2:0]			UsbAdpEna
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0593

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: ADP current probe timer

[7:4]	Reserved
[3:1]	**UsbAdpProbeTimeTh[2:0]** Threshold tolerance of UsbAdpTimeCurrent[10:0] measurement (that detect a new accessory Time = (UsbAdpProbeTimeTh[2:0] +2) x 32 kHz period (min: 62.5 µs, max: 281.5 µs)
[0]	**UsbAdpEna** 0: ADP is disabled 1: ADP is enabled

4.4.5 TVout registers

This information is not available in the public domain.

4.4.6 Accessory detection: Bank 8, Adr 10xxxxxx

AccDetectDb1Th — AccDetect debounce1

7	6	5	4	3	2	1	0
Reserved	AccDetect1Th[3:0]				AccDetectDb[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0880

Type: R/W

Reset: 0x78 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Accessory detection management.

[7]	Reserved
[6:3]	**AccDetect1Th[3:0]** Accessory Detection threshold on AccDetect1 ball 1000: 1.1 V 1001: 1.2 V 1010: 1.3 V 1011: 1.4 V 1100: 1.5 V 1101: 1.6 V 1110: 1.7 V 1111: 1.8 V
[2:0]	**AccDetectDb[2:0]** Under definition 000: 0 ms 001: 10 ms 010: 20 ms 011: 30 ms 100: 40 ms 101: 50 ms 110: 60 ms 111: 70 ms

AccDetect2Th — AccDetect debounce2

7	6	5	4	3	2	1	0
AccDetect22Th[3:0]				AccDetect21Th[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0881

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Accessory detection 2 management.

[7:4]	**AccDetect22Th[3:0]** 0000: 0.3 V 0001: 0.4 V 0010: 0.5 V 0011: 0.6 V 0100: 0.7 V 0101: 0.8 V 0110: 0.9 V 0111: 1.0 V 1000: 1.1 V 1001: 1.2 V 1010: 1.3 V 1011: 1.4 V 1100: 1.5 V 1101: 1.6 V 1110: 1.7 V 1111: 1.8 V
[3:0]	**AccDetect21Th[3:0]** 0000: 0.3 V 0001: 0.4 V 0010: 0.5 V 0011: 0.6 V 0100: 0.7 V 0101: 0.8 V 0110: 0.9 V 0111: 1.0 V 1000: 1.1 V 1001: 1.2 V 1010: 1.3 V 1011: 1.4 V 1100: 1.5 V 1101: 1.6 V 1110: 1.7 V 1111: 1.8 V

AccDetectCtrl AccDetectCtrl

7	6	5	4	3	2	1	0
Reserved		AccDetect22Ena	AccDetect21Ena	AccDetect2 PullUpEna	Reserved	VaccDetect2Pull UpSupEna	AccDetect1Ena
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: Address: 0x0882

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Accessory detection comparator management

[7:6]	Reserved
[5]	**AccDetect22Ena** Note: Does not turn On internal 2.1 V supply 0: Disable AccDetect22 comparator 1: Enable AccDetect22 comparator
[4]	**AccDetect21Ena** Note: Does not turn On internal 2.1 V supply 0: Disable AccDetect21 comparator 1: Enable AccDetect21 comparator
[3]	**AccDetect2PullUpEna** 0: Disable AccDetect2 Pull-up 1: Enable AccDetect2 Pull-up
[2]	Reserved
[1]	**VaccDetect2PullUpSupEna** 0: Disable 2.1 V supply for AccDetect2 Pull-up and AccDetect(i) comparator 1: Enable 2.1 V supply for AccDetect2 Pull-up and AccDetect(i) comparator
[0]	**AccDetect1Ena** Note: Does not turn On internal 2.1 V supply 0: Disable AccDetect1 comparator 1: Enable AccDetect1 comparator

4.4.7 GPADC: Bank 0x0A

GPADCCtrl1 GPADCCtrl1

7	6	5	4	3	2	1	0
IcharEna	BufEna	BTempPup SupSel	GPADCTrigEdge	BtempPullUp	ADCSwConvert	GPADCTrigEna	ADCEna
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0A00

Type: R/W (StdRegRstn, DigPORn, SwitchOffRstn)

Reset: 0b00X00000 (binary format)

Description: General purpose ADC management.

[7]	**IcharEna** 0: Disable ADC path charging current sense 1: Enable ADC path charging current sense
[6]	**BufEna** 0: Disable channel buffer 1: Enable channel buffer
[5]	**BtempPupSupSel (active only in PBT mode)** 0: Select TVout as Pull-Up supply 1: Select Vrtc as Pull-Up supply
[4]	**GPADCTrigEdge** 0: Select rising edge 1: Select falling edge
[3]	**BTempPullUp** 0: BatTemp ball pull-up is controlled by charger state machine 1: BatTemp ball pull-up is enabled
[2]	**ADCSwConvert** 0: Inactive 1: Launch an ADC conversion
[1]	**GPADCTrigEna** 0: disable GPADCTrig functionality 1: enable GPADCTrig functionality
[0]	**ADCEna** 0: Disable ADC 1: Enable ADC

GPADCCtrl2 GPADC Control

7	6	5	4	3	2	1	0
Reserved	ADCSwAverage[1:0]		ADCSwSel[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0A01

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: ADC input channel and number of measurement selection.

[7]	Reserved
[6:5]	**ADCSwAverage[1:0]** (define number of ADC sample to average) 00: 1 01: 4 10: 8 11: 16
[4:0]	**ADCSwSel[4:0]** (select ADC input channel) 00000: not used 00001: BatCtrl ball 00010: BatTemp ball 00011: Main Charger voltage 00100: AccDetect1 ball 00101: AccDetect2 ball 00110: AdcAux1 ball 00111: AdcAux2 ball 01000: VbatA ball 01001: Vbus Ball 01010: Main charger current 01011: USB charger current 01100: BackUpBat ball 01101: Reserved 01110: ID ball 01111: Internal test 1 10000: Internal test 2 10001: Internal test 3

GPADCCtrl3 GPADCCtrl3

7	6	5	4	3	2	1	0
Reserved	ADCHwAverage[1:0]		ADCHwSel[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0A02

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: ADC input channel and number of measurement selection when synchro is GPADCTrig ball

[7]	**Reserved**
[6:5]	**ADCHwAverage[1:0]:** (define number of ADC sample to average) 00: 1 01: 4 10: 8 11: 16
[4:0]	**ADCHwSel[4:0]** (select ADC input channel) 00000: Not used 00001: BatCtrl ball 00010: BatTemp ball 00011: Main Charger voltage 00100: AccDetect1 ball 00101: AccDetect2 ball 00110: AdcAux1 ball 00111: AdcAux2 ball 01000: VbatA ball 01001: Vbus Ball 01010: Main charger current 01011: USB charger current 01100: BackUpBat ball 01101: Reserved 01110: ID ball 01111: Internal test 1 10000: Internal test 2 10001: Internal test 3

GPADCTrigTimer GPADCTrigTimer

7	6	5	4	3	2	1	0
GPADCTrigTimer[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress+ 0x0A03

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPAC trigger delay timer

[7:0]	**GPADCTrigTimer[7:0]:** Defined GPADCTrig timer, from 0 to 255 x period of 32 kHz 00000000: 0 period 00000001: 1 period ..... 11111110: 254 periods 11111111: 255 periods

GPADCStatus GPADCStatus

7	6	5	4	3	2	1	0
							GPADCBusy
							R

Address: BaseAddress: 0x0A04

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: ADC status.

[7:1]	Reserved
[0]	**GPADCBusy** 0: GPADC not busy 1: GPADC is busy

GPADCSwDataL — GPADC Low Data byte in software mode

7	6	5	4	3	2	1	0
GPADCSwData[7:0]							
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0A05

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: ADC data management.

[7:0]	**GPADCSwData[7:0]** (ADC output data in manual mode)

GPADCSwDataH — GPADC High Data byte in software mode

7	6	5	4	3	2	1	0
Reserved						GPADCSwData[9:8]	
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0A06

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: ADC data management.

[7:2]	Reserved
[1:0]	**GPADCSwData[9:8]** (ADC output data in manual mode)

GPADCHwDataL — GPADC Data Low byte in ADCtrig mode

7	6	5	4	3	2	1	0
GPADCHwData[7:0]							
R	R	R	R	R	R	R	R

Address: Address: 0x0A07

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: ADC Data management when synchro is GPADCTrig ball

[7:0]	**GPADCHwData[7:0]** (ADC output data [7:0] in Hardware mode)

GPADCHwDataH — GPADC Data High byte in ADCtrig mode

7	6	5	4	3	2	1	0
Reserved						GPADCHwData[9:8]	
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0A08

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: ADC Data management when synchro is GPADCTrig ball

[7:2]	Reserved
[1:0]	**GPADCHwData[9:8]** (ADC output data [9:8] in Hardware mode)

4.4.8 Charger

This information is not available in the public domain.

4.4.9 Coulomb counter

This information is not available in the public domain.

4.4.10 Audio

All the registers of the 0x0Dxx bank are reset by the ‘ResetAudn’ bit [STw4500Ctrl3 register], or by the ‘SwReset’ bit [*AudSwReset* register]).

Figure 34 to *Figure 37* show where the registers are in the audio digital part.

Figure 34. Analog Blocks Registers

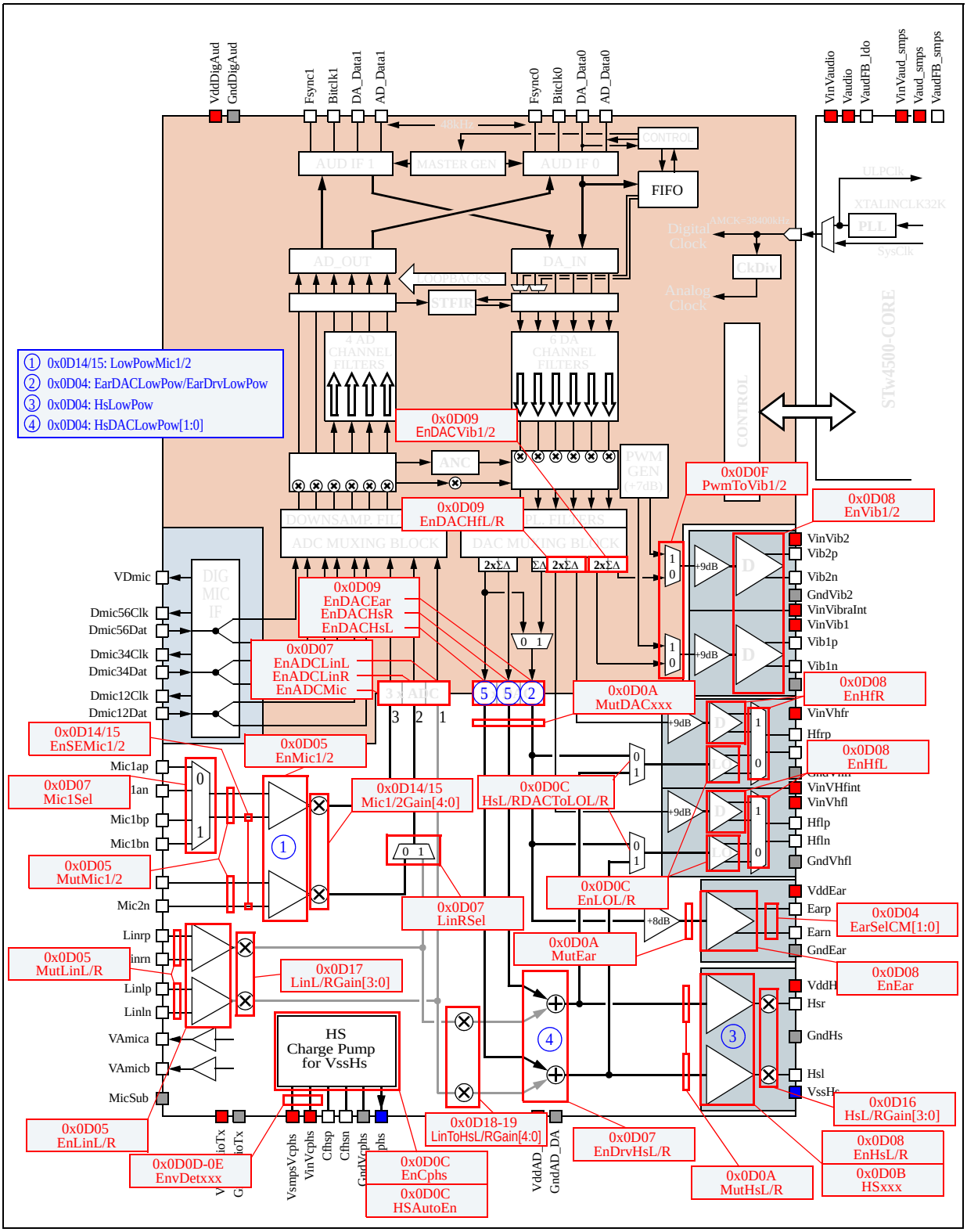


Figure 35. Digital AD and DA paths block Registers

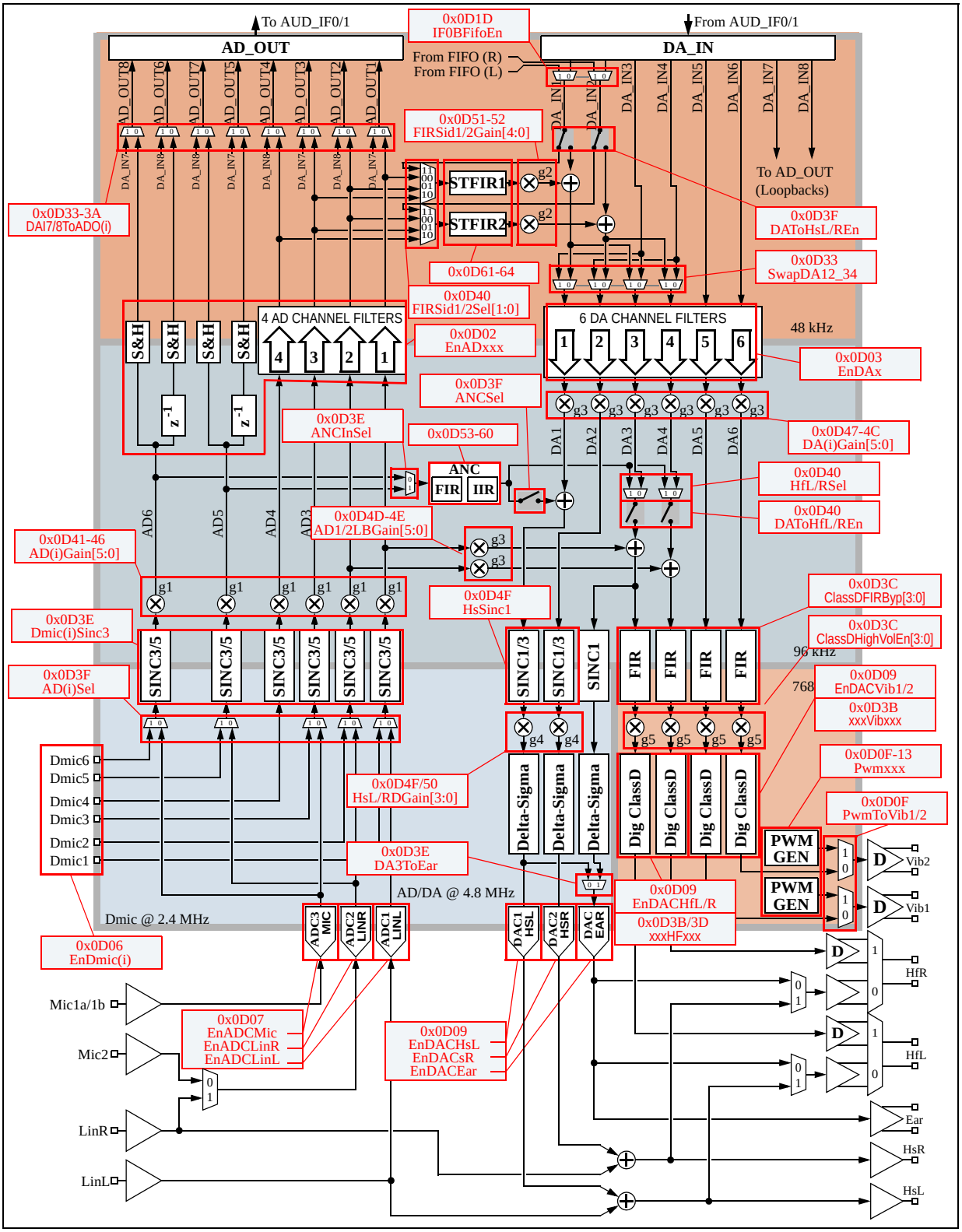


Figure 36. Audio Digital IF

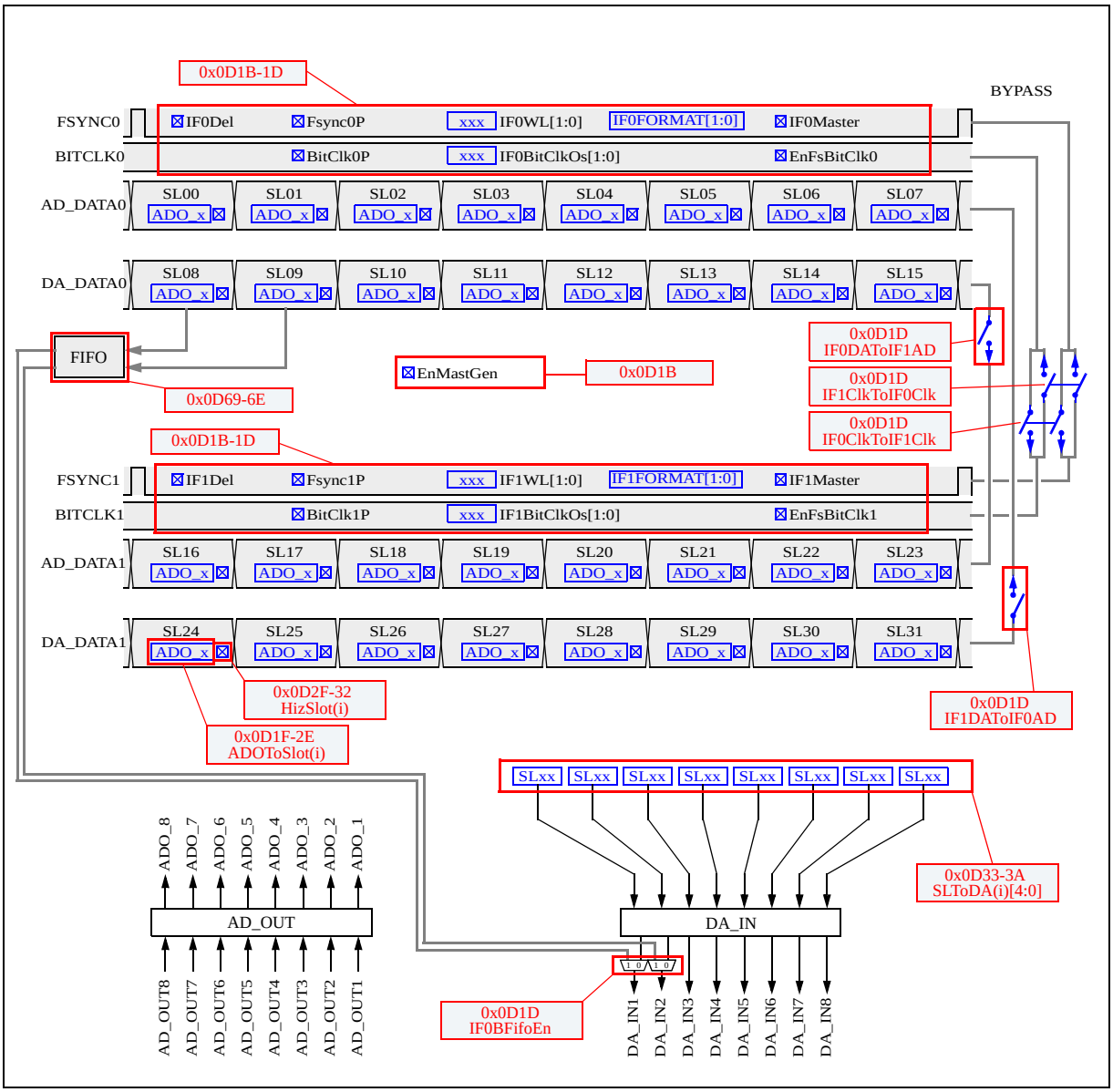
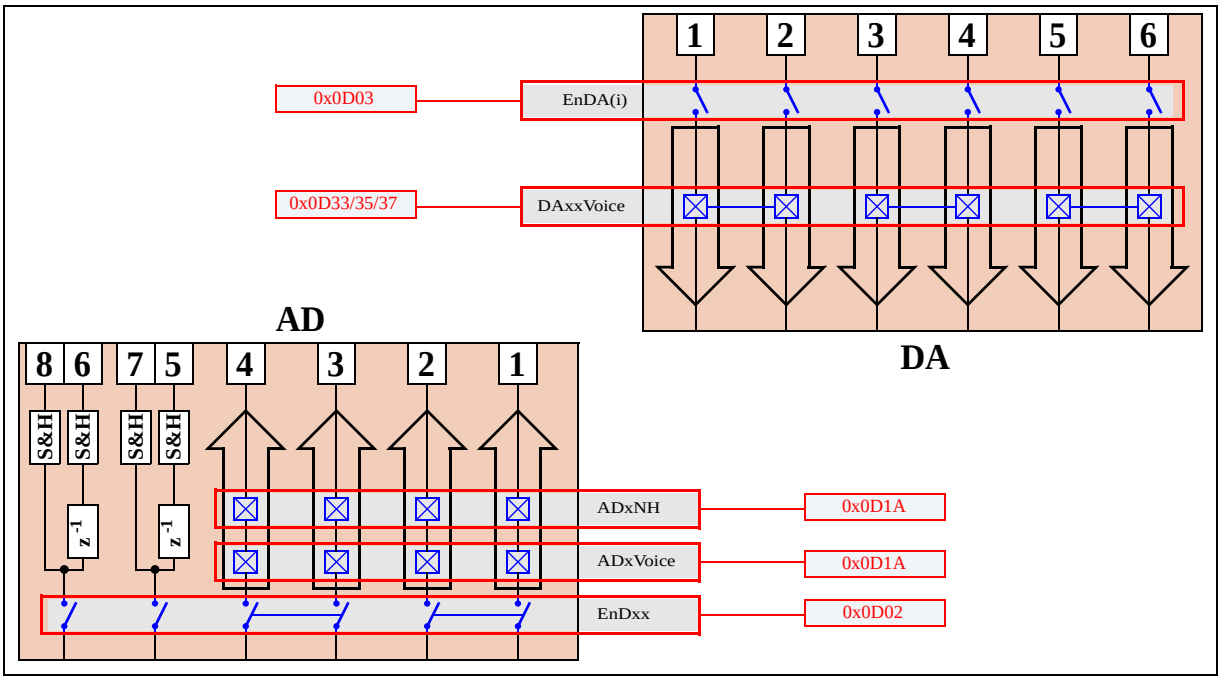


Figure 37. Digital Channel Filters Registers



General Power Up and Software reset

PowerUp — General power up

7	6	5	4	3	2	1	0
PowerUp	Reserved			EnAna	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D00

Type: R/W

Reset: 0x00

Description: General power up register.

[7]	**PowerUp** 0: The audio feature is in power down 1: The audio feature is in power up
[6:4]	Reserved
[3]	**EnAna** 0: All the audio analog parts are in power down 1: All the audio analog parts are in power up
[2:0]	Reserved

AudSwReset — Software Reset

7	6	5	4	3	2	1	0
SwReset	Reserved						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D01

Type: R/W

Reset: 0x00

Description: Software reset.

[7]	**SwReset** 0: Normal operation 1: Sets all the audio registers to their default state, including itself
[6:0]	Reserved

Digital Channels Enable

ADPathEna — Digital AD Channels Enable

7	6	5	4	3	2	1	0
EnAD12	Reserved	EnAD34	Reserved	EnAD5768	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D02

Type: R/W

Reset: 0x00

Description: Digital AD audio paths enable.

[7]	**EnAD12** 0: AD1 & AD2 paths are disabled 1: AD1 & AD2 paths are enabled
[6]	Reserved
[5]	**EnAD34** 0: AD3 & AD4 paths are disabled 1: AD3 & AD4 paths are enabled
[4]	Reserved
[3]	**EnAD5768** 0: AD5/7 & AD6/8 paths are disabled 1: AD5/7 & AD6/8 paths are enabled
[2:0]	Reserved

DAPathEna — Digital DA Channels Enable

7	6	5	4	3	2	1	0
EnDA1	EnDA2	EnDA3	EnDA4	EnDA5	EnDA6	EnHpEar	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D03

Type: R/W

Reset: 0x00

Description: Digital DA audio paths enable.

[7]	**EnDA1** 0: DA1 path is disabled 1: DA1 path is enabled
[6]	**EnDA2** 0: DA2 path is disabled 1: DA2 path is enabled
[5]	**EnDA3** 0: DA3 path is disabled 1: DA3 path is enabled
[4]	**EnDA4** 0: DA4 path is disabled 1: DA4 path is enabled
[3]	**EnDA5** 0: DA5 path is disabled 1: DA5 path is enabled
[2]	**EnDA6** 0: DA6 path is disabled 1: DA6 path is enabled
[1]	**EnHpEar** 0: High Pass filter for earpiece is disabled 1: High Pass filter for earpiece is enabled
[0]	Reserved

Analog and Dmic Controls

AnaConf1 — Low Power and HS/Ear configuration

7	6	5	4	3	2	1	0
HsLowPow	HsDACLowPow[1:0]		EarDACLowPow	EarSelCM[1:0]		HsHpEn	EarDrvLowPow
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D04

Type: R/W

Reset: 0x00

Description: Low Power and Headset/earp amp configuration.

[7]	**HsLowPow** 0: Normal Operation 1: Hs drivers in Low Power
[6:5]	**HsDACLowPow[1:0]** 00: Normal Operation 01: Hs DAC drivers in Low Power 10: Hs DAC in Low Power 11: Hs DAC and Hs DAC drivers in Low Power
[4]	**EarDACLowPow** 0: Normal Operation 1: Ear DAC in Low Power
[3:2]	**EarSelCM[1:0]** 00: Nominal common mode for Ear driver 0.95 V 01: Nominal common mode for Ear driver 1.1 V 10: Nominal common mode for Ear driver 1.27 V 11: Nominal common mode for Ear driver 1.58 V
[1]	**HsHpEn** Offset cancellation for Headset driver. 0: Headset high pass filter disabled 1: Headset high pass filter enabled (offset cancellation enabled)
[0]	**EarDrvLowPow** 0: Normal Operation 1: Ear DAC driver in Low Power

AnaConf2 — Line in Conf

7	6	5	4	3	2	1	0
EnMic1	EnMic2	EnLinL	EnLinR	MutMic1	MutMic2	MutLinL	MutLinR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D05

Type: R/W

Reset: 0x0F

Description: Line in and microphone configurations.

[7]	**EnMic1** 0: Mic1A and Mic1B microphone amplifier is in power down 1: Mic1A (‘Mic1Sel’=0) or Mic1B (‘Mic1Sel’=1) microphone amplifier is in power up Note: ‘Mic1sel’ bit (*AnaConf3* register)
[6]	**EnMic2** 0: Mic2 microphone is in power down 1: Mic2 microphone is in power up
[5]	**EnLinL** 0: Line-in left input is in power down 1: Line-in left input is in power up
[4]	**EnLinR** 0: Line-in right input is in power down 1: Line-in right input is in power up
[3]	**MutMic1** 0: Analog microphone Mic1A/B input is active 1: Analog microphone Mic1A/B input is muted
[2]	**MutMic2** 0: Analog microphone Mic2 input is active 1: Analog microphone Mic2 input is muted
[1]	**MutLinL** 0: Analog Line-In L input is active 1: Analog Line-In L input is muted
[0]	**MutLinR** 0: Analog Line-In R input is active 1: Analog Line-In R input is muted

DigMicConf — Digital mic inputs enable

7	6	5	4	3	2	1	0
EnDmic1	EnDmic2	EnDmic3	EnDmic4	EnDmic5	EnDmic6	HsFadSpeed[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D06

Type: R/W

Reset: 0x00

Description: Digital Inputs Enable.

[7]	**EnDmic1** 0: Dmic1 input is muted 1: Dmic1 input is active and Dmic12Clk is running
[6]	**EnDmic2** 0: Dmic2 input is muted 1: Dmic2 input is active and Dmic12Clk is running
[5]	**EnDmic3** 0: Dmic3 input is muted 1: Dmic3 input is active and Dmic34Clk is running
[4]	**EnDmic4** 0: Dmic4 input is muted 1: Dmic4 input is active and Dmic34Clk is running
[3]	**EnDmic5** 0: Dmic5 input is muted 1: Dmic5 input is active and Dmic56Clk is running
[2]	**EnDmic6** 0: Dmic6 input is muted 1: Dmic6 input is active and Dmic56Clk is running
[1:0]	**HsFadSpeed[1:0]** Approximate time between each 2/4 dB Headset gain step 00: 2 ms 01: 0.5 ms 10: 10.6 ms 11: 5 ms The fade speed applies to analog HsL and HsR gains, the automatic fading gain can be disabled with HsFadDis bit (*ShortCirConf* register)

AnaConf3 ADC Enable

7	6	5	4	3	2	1	0
Mic1Sel	LinRSel	EnDrvHsL	EnDrvHsR	Reserved	EnADCMic	EnADCLinL	EnADCLinR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D07

Type: R/W

Reset: 0x00

Description: Analog to Digital Converters Enable and DAC drivers enable.

[7]	**Mic1Sel** 0: ADC3 connected to Mic1A while Mic1B input is power down 1: ADC3 connected to Mic1B while Mic1A input is power down
[6]	**LinRSel** 0: ADC2 connected to Mic2 1: ADC2 connected to LinR
[5]	**EnDrvHsL** 0: HsL Dac driver is power down 1: HsL Dac driver is power up
[4]	**EnDrvHsR** 0: HsR Dac driver is power down 1: HsR Dac driver is power up
[3]	Reserved
[2]	**EnADCMic** 0: ADC3 is power down 1: ADC3 is power-up
[1]	**EnADCLinL** 0: ADC1 is power down 1: ADC1 is power-up
[0]	**EnADCLinR** 0: ADC2 is power down 1: ADC2 is power up

AnaConf4 Analog Output Enable

7	6	5	4	3	2	1	0
DisPdVss	EnEar	EnHsL	EnHsR	EnHfL	EnHfR	EnVib1	EnVib2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D08

Type: R/W

Reset: 0x00

Description: Analog Output Enable.

[7]	**DisPdVss** 0: Internal pull down on VssVcphs is enabled. 1: Internal pull down on VssVcphs is disabled.
[6]	**EnEar** 0: The Ear Class-AB driver is powered down 1: The Ear Class-AB driver is powered up
[5]	**EnHsL** 0: The HsL Driver is powered down 1: The HsL Driver is powered up
[4]	**EnHsR** 0: The HsR Driver is powered down 1: The HsR Driver is powered up
[3]	**EnHfL** 0: The HfL Class-D driver is powered down 1: The HfL Class-D driver is powered up
[2]	**EnHfR** 0: The HfR Class-D driver is powered down 1: The HfR Class-D driver is powered up
[1]	**EnVib1** 0: The Vib1 Class-D driver is powered down 1: The Vib1 Class-D driver is powered up
[0]	**EnVib2** 0: The Vib2 Class-D driver is powered down 1: The Vib2 Class-D driver is powered up

DAPathConf — Digital Output Enable

7	6	5	4	3	2	1	0
CPLowFreq LimEn	EnDACEar	EnDACHsL	EnDACHsR	EnDACHfL	EnDACHfR	EnDACVib1	EnDACVib2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D09

Type: R/W

Reset: 0x00

Description: Digital Output Enable.

[7]	**CPLowFreqLimEn** 0: Negative charge pump works in normal mode 1: Negative charge pump frequency cannot be in audio band
[6]	**EnDACEar** 0: Ear DAC and digital dedicated path are powered down 1: Ear DAC and digital dedicated path are powered up
[5]	**EnDACHsL** 0: HsL DAC and digital dedicated path are powered down 1: HsL DAC and digital dedicated path are powered up
[4]	**EnDACHsR** 0: HsR DAC and digital dedicated path are powered down 1: HsR DAC and digital dedicated path are powered up
[3]	**EnDACHfL** 0: HfL digital class D plus dedicated digital path are powered down 1: HfL digital class D plus dedicated digital path are powered up
[2]	**EnDACHfR** 0: HfR digital class D plus dedicated digital path are powered down 1: HfR digital class D plus dedicated digital path are powered up
[1]	**EnDACVib1** 0: Vib1 digital class D plus dedicated digital path are power down 1: Vib1 digital class D plus dedicated digital path are powered up
[0]	**EnDACVib2** 0: Vib2 digital class D plus dedicated digital path are powered down 1: Vib2 digital class D plus dedicated digital path are powered up

MuteConf — Mute Enable

7	6	5	4	3	2	1	0
Reserved	MutEar	MutHsL	MutHsR	Reserved	MutDACEar	MutDACHsL	MutDACHsR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D0A

Type: R/W

Reset: 0x77

Description: Mute enable.

[7]	Reserved
[6]	**MutEar** 0: The Ear driver is in normal mode 1: The Ear driver is muted
[5]	**MutHsL** 0: The HsL driver is in normal mode 1: The HsL Driver is muted
[4]	**MutHsR** 0: The HsR Driver is in normal mode 1: The HsR Driver is muted
[3]	Reserved
[2]	**MutDACEar** 0: The Ear DAC is in normal mode 1: The Ear DAC is muted
[1]	**MutDACHsL** 0: The HsL DAC is in normal mode 1: The HsL DAC is muted
[0]	**MutDACHsR** 0: The HsR DAC is in normal mode 1: The HsR DAC is muted

ShortCirConf — Short Circuit Disable

7	6	5	4	3	2	1	0
EnShortPWD	EarShortDis	HsShortDis	HsPullDEn	Reserved	HsOscEn	HsFadDis	HsZcdDis
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D0B

Type: R/W

Reset: 0x00

Description: Short circuit disable

[7]	**EnShortPWD** This bit acts on the Earpiece and Headset driver 0: Automatic switch off on short circuit detection is disabled 1: Automatic switch off on short circuit detection is enabled
[6]	**EarShortDis** 0: Short circuit detection on Ear driver enabled 1: Short circuit detection on Ear driver disabled
[5]	**HsShortDis** 0: Short circuit detection on HsL and HsR drivers enabled 1: Short circuit detection on HsL and HsR drivers disabled
[4]	**HsPullDEn** 0: HsL and HsR outputs are in high impedance 1: HsL and HsR outputs are pulled down to ground
[3]	Reserved
[2]	**HsOscEn** 0: The HS drivers use the system clock 1: The HS drivers use a local oscillator (system clock absent: analog path only)
[1]	**HsFadDis** 0: All intermediate steps are applied between two programmed gains (fading) 1: Gain on HS is applied immediately
[0]	**HsZcdDis** 0: HS gain changes on signal zero cross (unless time-out occurs) 1: HS gain is changed without zero cross control

AnaConf5 NCP enable, HS autostart

7	6	5	4	3	2	1	0
EnCpHs	Reserved	HsLDACToLOL	HsRDACToLOR	EnLOL	EnLOR	Reserved	HsAutoEn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D0C

Type: R/W

Reset: 0x00

Description: NCP enable, HS autostart.

[7]	**EnCpHs** 0: Negative Charge Pump disabled. 1: Negative Charge Pump enabled.
[6]	Reserved
[5]	**HsLDACToLOL** 0: Left Line-Out driver input is Ear-DAC. 1: Left Line-Out driver input is HsL-DAC.
[4]	**HsRDACToLOR** 0: Right Line-Out driver input is Ear-DAC. 1: Right Line-Out driver input is HsR-DAC.
[3]	**EnLOL** 0: Left Line-Out driver is disabled. 1: Left Line-Out driver is enabled (if EnHfL=0 in *AnaConf4* register).
[2]	**EnLOR** 0: Right Line-Out driver is disabled. 1: Right Line-Out driver is enabled (if EnHfR=0 in *AnaConf4* register).
[1]	Reserved
[0]	**HsAutoEn** 0: HS drivers and NCP are enabled/disabled with bits EnHsL/R and EnCpHs 1: HS drivers and NCP can be fully controlled with EnCpHs bit(1)

1. Automatic Fast Startup of HS-drivers/NCP system sequence:
   a) set 'HsAutoEn' = 1
   b) set bits 'EnHsL' and 'EnHsR' = 1
   c) set 'EnCpHs' = 1; with this bit the charge pump is enabled and when the output voltage is valid (bit 'IT_VssReady'=1) the headset drivers are actually enabled.

   Automatic Fast Shutdown of headset drivers/NCP system sequence:
   d) set 'EnCpHs' = 0; with this bit the headset drivers shutdown sequence is started, when the drivers are off the NCP is actually powered down.
   e) set bits 'EnHsL' and 'EnHsR' = 0
   f) set 'HsAutoEn' = 0

Envelope Control

EnvCPConf — Envelope Thresholds

7	6	5	4	3	2	1	0
EnvDetHThre[3:0]				EnvDetLThre[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D0D

Type: R/W

Reset: 0x00

Description: Threshold of envelope detection.

[7:4]	**EnvDetHThre[3:0]**[(1)] High threshold for Charge Pump Low Voltage selection (Measured at HS output) 0000: 25mV 0001: 50mV 0010: 100mV .....: 50mV step 1110: 700mV 1111: 750mV
[3:0]	**EnvDetLThre[3:0]** Low threshold for Charge Pump input switch 0000: 25mV 0001: 50mV 0010: 100mV .....: 50mV step 1110: 700mV 1111: 750mV

1. The threshold is measured in the digital DAC path, then it takes into account all the DAC path gain to provide a threshold value that can be measured at the headset driver output. For this reason the envelope detection cannot take into account line-in to headset analog mixing.

SigEnvConf — Envelope Decay Time

7	6	5	4	3	2	1	0
Reserved		CpLVEn	EnvDetCpEn	EnvDetTime[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D0E

Type: R/W

Reset: 0x00

Description: Decay time of envelope detection.

[7:6]	Reserved
[5]	**CpLVEn** Input voltage control for Charge Pump. Active just when envelope detection is disabled. 0: VinVcphs ball supplies negative charge Pump. 1: SmpsVcphs ball supplies negative charge Pump.
[4]	**EnvDetCpEn** 0: Envelope detection for charge pump disabled. 1: Envelope detection for charge pump enabled.
[3:0]	**EnvDetTime[3:0]** Decay time for envelope detection 0000: 27usec 0001: 53usec 0010: 106usec n: 26.6 µs*2^n 1110: 436msec 1111: 872msec

Class-D and PWM-generator control

PWMGenConf1 — Class-D Configuration

7	6	5	4	3	2	1	0
PwmToVib1	PwmToVib2	Pwm1Ctrl	Pwm2Ctrl	Pwm1nCtrl	Pwm1pCtrl	Pwm2nCtrl	Pwm2pCtrl
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D0F

Type: R/W

Reset: 0x00

Description: Configuration of class-D drivers.

[7]	**PwmToVib1** 0: Vib1 driver is connected to corresponding DA path 1: Vib1 driver is controlled by internal Pwm Generator
[6]	**PwmToVib2** 0: Vib2 driver is connected to corresponding DA path 1: Vib2 driver is controlled by internal Pwm Generator
[5]	**Pwm1Ctrl** When Pwm1 generator is enable Vib1 andVib2 are started together (used in differential) 0: Pwm generator is controlled by ‘PwmVib1nPol’ and ‘PwmVib1pPol’ bit values 1: Pwm generator is controlled by ‘PwmVib1nDutCyc[6:0]’ and ‘PwmVib1pDutCyc[6:0]’ bit values
[4]	**Pwm2Ctrl** When Pwm2 generator is enable positive and negative are started together (used in differential) 0: Pwm generator is controlled by ‘PwmVib2nPol’ and ‘PwmVib2pPol’ bit value 1: Pwm generator is controlled by ‘PwmVib2nDutCyc[6:0]’ bit value
[3]	**Pwm1nCtrl** When Pwm1 generator is enable negative is started separately from positive (not used in differential) 0: Pwm generator is controlled by ‘PwmVib1nPol’ bit value 1: Pwm generator is controlled by ‘PwmVib1nDutCyc[6:0]’ bit value
[2]	**Pwm1pCtrl** When Pwm1 generator is enable positive is started separately from negative (not used in differential) 0: Pwm generator is controlled by ‘PwmVib1pPol’ bit value 1: Pwm generator is controlled by ‘PwmVib1pDutCyc[6:0]’ bit value
[1]	**Pwm2nCtrl** When Pwm2 generator is enable negative is started separately from positive (not used in differential) 0: Pwm generator is controlled by ‘PwmVib2nPol’ bit value 1: Pwm generator is controlled by ‘PwmVib2nDutCyc[6:0]’ bit value
[0]	**Pwm2pCtrl** When Pwm2 generator is enable positive is started separately from negative (not used in differential) 0: Pwm generator is controlled by ‘PwmVib2pPol’ bit value 1: Pwm generator is controlled by ‘PwmVib2pDutCyc[6:0]’ bit value

PWMGenConf2 — Pwm Vib1n Configuration

7	6	5	4	3	2	1	0
PwmVib1pPol	PwmVib1pDutCyc[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D10

Type: R/W

Reset: 0x32

Description: Configuration of negative Pwm output for Vib1 class-D driver.

[7]	**PwmVib1pPol** 0: Vib1p ball is forced to GndVib voltage 1: Vib1p ball is forced to VinVib voltage
[6:0]	**PwmVib1pDutCyc[6:0]**(1) 0000000: Duty cycle is 0% 0000001: Duty cycle is 1% .....: 1% step 1100011: Duty cycle is 99% 1100100 to 1111111: Duty cycle is 100%

1. The PWM modulation duty cycle described in the control register does not directly correspond to the PWM modulation duty cycle at the Vib output. See *Section : HF and Vib digital power outputs* for details.

PWMGenConf3 — Pwm Vib1p Configuration

7	6	5	4	3	2	1	0
PwmVib1nPol	PwmVib1nDutCyc[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D11

Type: R/W

Reset: 0x32

Description: Configuration of positive Pwm output for Vib1 class-D driver.

[7]	**PwmVib1nPol** 0: Vib1n ball is forced to GndVib voltage 1: Vib1n ball is forced to VinVib voltage
[6:0]	**PwmVib1nDutCyc[6:0]**(1) 0000000: Duty cycle is 0% 0000001: Duty cycle is 1% .....: 1% step 1100011: Duty cycle is 99% 1100100 to 1111111: Duty cycle is 100%

1. The PWM modulation duty cycle described in the control register does not directly correspond to the PWM modulation duty cycle at the Vib output. See *Section : HF and Vib digital power outputs* for details.

PWMGenConf4 Pwm Vib2n Configuration

7	6	5	4	3	2	1	0
PwmVib2pPol	PwmVib2pDutCyc[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D12

Type: R/W

Reset: 0x32

Description: Configuration of negative Pwm output for Vib2 class-D driver.

[7]	**PwmVib2pPol** 0: Vib2p ball is forced to GndVib voltage 1: Vib2p ball is forced to VinVib voltage
[6:0]	**PwmVib2pDutCyc[6:0]**(1) 0000000: Duty cycle is 0% 0000001: Duty cycle is 1% .....: 1% step 1100011: Duty cycle is 99% 1100100 to 1111111: Duty cycle is 100%

1. The PWM modulation duty cycle described in the control register does not directly correspond to the PWM modulation duty cycle at the Vib output. See *Section : HF and Vib digital power outputs* for details..

PWMGenConf5 Pwm Vib2p Configuration

7	6	5	4	3	2	1	0
PwmVib2nPol	PwmVib2nDutCyc[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D13

Type: R/W

Reset: 0x32

Description: Configuration of positive Pwm output for Vib2 class-D driver.

[7]	**PwmVib2nPol** 0: Vib2n ball is forced to GndVib voltage 1: Vib2n ball is forced to VinVib voltage
[6:0]	**PwmVib2nDutCyc[6:0]**(1) 0000000: Duty cycle is 0% 0000001: Duty cycle is 1% .....: 1% step 1100011: Duty cycle is 99% 1100100 to 1111111: Duty cycle is 100%

1. The PWM modulation duty cycle described in the control register does not directly correspond to the PWM modulation duty cycle at the Vib output. See *Section : HF and Vib digital power outputs* for details

Analog Gains

AnaGain1 — Microphone 1 Gain

7	6	5	4	3	2	1	0
EnSEMic1	LowPowMic1	Reserved	Mic1Gain[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D14

Type: R/W

Reset: 0x00

Description: Gain for Microphone 1A or 1B.

[7]	**EnSEMic1** 0: Differential microphone is connected to Mic1A or Mic1B inputs 1: Single ended microphone is connected to Mic1A or Mic1B inputs
[6]	**LowPowMic1** 0: Normal Operation 1: Microphone Preamplifier 1 is in Low Power
[5]	Reserved
[4:0]	**Mic1Gain[4:0]** Mic1A or Mic1B Analog Gain 00000: 0 dB gain 00001: 1 dB gain .....: + 1 dB step 11101: 29 dB gain 11110: 30 dB gain 11111: 31 dB gain

AnaGain2 — Microphone 2 Gain

7	6	5	4	3	2	1	0
EnSEMic2	LowPowMic2	Reserved	Mic2Gain[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D15

Type: R/W

Reset: 0x00

Description: Gain for Microphone 2.

[7]	**EnSEMic2** 0: Differential microphone is connected to Mic2 inputs 1: Single ended microphone is connected to Mic2 inputs
[6]	**LowPowMic2** 0: Normal Operation 1: Microphone Preamplifier 2 is in Low Power
[5]	Reserved
[4:0]	**Mic2Gain[4:0]** Mic2 Analog Gain 00000: 0 dB gain 00001: 1 dB gain .....: +1 dB step 11101: 29 dB gain 11110: 30 dB gain 11111: 31 dB gain

AnaGain3 — Left line-in and Hs Analog Gain

7	6	5	4	3	2	1	0
HsLGain[3:0]				HsRGain[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D16

Type: R/W

Reset: 0xFF

Description: Gain for Left and right Headset analog gain.

[7:4]	**HsLGain[3:0]** Left headset analog gain 0000: +4 dB gain 0001: +2 dB gain .....: -2 dB step 1011: -18 dB gain 1100: -20 dB gain 1101: -24 dB gain 1110: -28 dB gain 1111: -32 dB gain
[3:0]	**HsRGain[3:0]** Right headset analog gain 0000: +4 dB gain 0001: +2 dB gain .....: -2 dB step 1011: -18 dB gain 1100: -20 dB gain 1101: -24 dB gain 1110: -28 dB gain 1111: -32 dB gain

AnaGain4 — Right line-in and Hs Analog Gain

7	6	5	4	3	2	1	0
LinLGain[3:0]				LinRGain[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D17

Type: R/W

Reset: 0x55

Description: Left and Right Line-In analog gain.

[7:4]	**LinLGain[3:0]** Left line-in gain 0000: -10 dB gain 0001: -8 dB gain .....: 2 dB step 0101: 0 dB gain .....: 2 dB step 1110: 18 dB gain 1111: 20 dB gain
[3:0]	**LinRGain[3:0]** Right line-in gain 0000: -10 dB gain 0001: -8 dB gain .....: 2 dB step 0101: 0 dB gain .....: 2 dB step 1110: 18 dB gain 1111: 20 dB gain

DigLinHsLGain — Line-in to HsL Gain

7	6	5	4	3	2	1	0
Reserved			LinToHsLGain[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D18

Type: R/W

Reset: 0x1F

Description: Line-In to Headset left gain.

[7:5]	Reserved
[4:0]	**LinToHsLGain[4:0]** Line-in to headset left gain 00000: 0 dB gain 00001: -2 dB gain .....: -2 dB step 10001: -34 dB gain 10010: -36 dB gain 10011 to 11111: - inf dB gain

DigLinHsRGain — Line-in to HsR Gain

7	6	5	4	3	2	1	0
Reserved			LinToHsRGain[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D19

Type: R/W

Reset: 0x1F

Description: Line-In to Headset right gain.

[7:5]	Reserved
[4:0]	**LinToHsRGain[4:0]** Line-in to headset right gain 00000: 0 dB gain 00001: -2 dB gain .....: -2 dB step 10001: -34 dB gain 10010: -36 dB gain 10011 to 11111: -inf dB gain

AD DSP paths control

ADFiltConf — AD Channel Filters Configuration

7	6	5	4	3	2	1	0
AD1NH	AD2NH	AD3NH	AD4NH	AD1Voice	AD2Voice	AD3Voice	AD4Voice
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D1A

Type: R/W

Reset: 0x00

Description: Audio and Voice filters configuration for AD paths.

[7]	**AD1NH** 0: AD1 Path with audio Offset Cancellation filter enabled 1: AD1 Path with audio Offset Cancellation filter disabled
[6]	**AD2NH** 0: AD2 Path with audio Offset Cancellation filter enabled 1: AD2 Path with audio Offset Cancellation filter disabled
[5]	**AD3NH** 0: AD3 Path with audio Offset Cancellation filter enabled 1: AD3 Path with audio Offset Cancellation filter disabled
[4]	**AD4NH** 0: AD4 Path with audio Offset Cancellation filter enabled 1: AD4 Path with audio Offset Cancellation filter disabled
[3]	**AD1Voice** 0: AD1 channel path use Audio Filters 1: AD1 channel path use 48 kHz Low Latency Filters for Voice
[2]	**AD2Voice** 0: AD2 channel path use Audio Filters 1: AD2 channel path use 48 kHz Low Latency Filters for Voice
[1]	**AD3Voice** 0: AD3 channel path use Audio Filters 1: AD3 channel path use 48 kHz Low Latency Filters for Voice
[0]	**AD4Voice** 0: AD4 channel path use Audio Filters 1: AD4 channel path use 48 kHz Low Latency Filters for Voice

TDM Audio Interface Control

DigIFConf1 — TDM Configuration

7	6	5	4	3	2	1	0
EnMastGen	IF1BitClkOs[1:0]		EnFsBitClk1	Reserved	IF0BitClkOs[1:0]		EnFsBitClk0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D1B

Type: R/W

Reset: 0x00

Description: Audio interface 0/1 master configuration.

[7]	**EnMastGen** 0: The Master Generator for AUD_IF1/0 is stopped 1: The Master Generator for AUD_IF1/0 is active
[6:5]	**IF1BitClkOs[1:0]** BitClk1 = 48 kHz x N 00: N = 32 01: N = 64 10: N = 128 11: N = 256
[4]	**EnFsBitClk1** 0: The FSync1 and BitClk1 bits are stopped 1: The FSync1 and BitClk1 bits are enabled
[3]	Reserved
[2:1]	**IF0BitClkOs[1:0]** BitClk0 = 48kHz x N 00: N = 32 01: N = 64 10: N = 128 11: N = 256
[0]	**EnFsBitClk0** 0: The FSync0 and BitClk0 bits are stopped 1: The FSync0 and BitClk0 bits are enabled

DigIFConf2 TDM Configuration

7	6	5	4	3	2	1	0
Reserved	Fsync0P	BitClk0P	IF0Del	IF0Format[1:0]		IF0WL[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D1C

Type: R/W

Reset: 0x02

Description: TDM Configuration.

[7]	Reserved
[6]	**Fsync0P** 0: The first slot of AUD_IF0 is synchronized with Fsync rising edge 1: The first slot of AUD_IF0 is synchronized with Fsync falling edge
[5]	**BitClk0P** 0: The input bits of AUD_IF0 are sampled with BitClk rising edge 1: The input bits of AUD_IF0 are sampled with BitClk falling edge
[4]	**IF0Del** 0: IF0 format is not delayed 1: IF0 format is delayed
[3:2]	**IF0Format[1:0]** 00: IF0 is disabled (no data is read from the interface). 01: IF0 format is TDM 1x: IF0 format is I2S Left Aligned
[1:0]	**IF0WL[1:0]** 00: IF0 Word Length is 16 bits 01: IF0 Word Length is 20 bits 10: IF0 Word Length is 24 bits 11: IF0 Word Length is 32 bits

DigIFConf3 — TDM bypass control

7	6	5	4	3	2	1	0
IF0DAToIF1AD	IF0ClkToIF1Clk	IF1Master	Reserved	IF1DAToIF0AD	IF1ClkToIF0Clk	IF0Master	IF0BFifoEn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D1D

Type: R/W

Reset: 0x00

Description: TDM bypass control

[7]	**IF0DAToIF1AD** 0: AD_Data1 ball is used for the default purpose 1: Data on DA_Data0 ball is sent to AD_Data1 ball
[6]	**IF0ClkToIF1Clk** 0: BitClk1, Fsync1 balls are used for the default purpose 1: Clocks on BitClk0, Fsync0 balls are sent to BitClk1, Fsync1 balls
[5]	**IF1Master** 0: Balls FSync1 and BitClk1 are set as input 1: Balls FSync1 and BitClk1 are set as output
[4]	Reserved
[3]	**IF1DAToIF0AD** 0: AD_Data0 ball is used for the default purpose 1: Data on DA_Data1 ball is sent to AD_Data0 ball
[2]	**IF1ClkToIF0Clk** 0: BitClk0, Fsync0 balls are used for the default purpose 1: Clocks on BitClk1,Fsync1 balls are sent to BitClk0, Fsync0 balls
[1]	**IF0Master** 0: Balls FSync0 and BitClk0 are set as input 1: Balls FSync0 and BitClk0 are set as output
[0]	**IF0BFifoEn** 0: TDM interface IF0 is configured in normal mode 1: TDM interface IF0 is configured in burst mode

DigIFConf4 TDM format

7	6	5	4	3	2	1	0
Reserved	Fsync1P	BitClk1P	IF1Del	IF1Format[1:0]		IF1WL[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D1E

Type: R/W

Reset: 0x02

Description: Audio interface 1 configuration

[7]	Reserved
[6]	**Fsync1P** 0: The first slot of AUD_IF1 is synchronized with Fsync rising edge 1: The first slot of AUD_IF1 is synchronized with Fsync falling edge
[5]	**BitClk1P** 0: The input bits of AUD_IF1 are sampled with BitClk rising edge 1: The input bits of AUD_IF1 are sampled with BitClk falling edge
[4]	**IF1Del** 0: IF1 format is not delayed 1: IF1 format is delayed
[3:2]	**IF1Format[1:0]** 00: IF1 is disabled (no data is read from the interface) 01: IF1 format is TDM 1x: IF1 format is I2S Left Aligned
[1:0]	**IF1WL[1:0]** 00: IF1 Word Length is 16 bits 01: IF1 Word Length is 20 bits 10: IF1 Word Length is 24 bits 11: IF1 Word Length is 32 bits

TDM Audio Interface slots assignment from AD path

ADSlotSel1 — AD Data allocation in Slot 0 to 1

7	6	5	4	3	2	1	0
ADOToSlot1[3:0]				ADOToSlot0[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D1F

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 0 to 1

[7:4]	**ADOToSlot1[3:0]** 0000: Slot 01 outputs data from AD_OUT1 0001: Slot 01 outputs data from AD_OUT2 0010: Slot 01 outputs data from AD_OUT3 0011: Slot 01 outputs data from AD_OUT4 0100: Slot 01 outputs data from AD_OUT5 0101: Slot 01 outputs data from AD_OUT6 0110: Slot 01 outputs data from AD_OUT7 0111: Slot 01 outputs data from AD_OUT8 10xx: Slot 01 outputs zeros 11xx: Slot 01 is tristate
[3:0]	**ADOToSlot0[3:0]** 0000: Slot 00 outputs data from AD_OUT1 0001: Slot 00 outputs data from AD_OUT2 0010: Slot 00 outputs data from AD_OUT3 0011: Slot 00 outputs data from AD_OUT4 0100: Slot 00 outputs data from AD_OUT5 0101: Slot 00 outputs data from AD_OUT6 0110: Slot 00 outputs data from AD_OUT7 0111: Slot 00 outputs data from AD_OUT8 10xx: Slot 00 outputs zeros 11xx: Slot 00 is tristate

ADSlotSel2 — AD Data allocation in Slot 2 to 3

7	6	5	4	3	2	1	0
ADOToSlot3[3:0]				ADOToSlot2[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D20

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 2 to 3

[7:4]	**ADOToSlot3[3:0]** 0000: Slot 03 outputs data from AD_OUT1 0001: Slot 03 outputs data from AD_OUT2 0010: Slot 03 outputs data from AD_OUT3 0011: Slot 03 outputs data from AD_OUT4 0100: Slot 03 outputs data from AD_OUT5 0101: Slot 03 outputs data from AD_OUT6 0110: Slot 03 outputs data from AD_OUT7 0111: Slot 03 outputs data from AD_OUT8 10xx: Slot 03 outputs zeros 11xx: Slot 03 is tristate
[3:0]	**ADOToSlot2[3:0]** 0000: Slot 02 outputs data from AD_OUT1 0001: Slot 02 outputs data from AD_OUT2 0010: Slot 02 outputs data from AD_OUT3 0011: Slot 02 outputs data from AD_OUT4 0100: Slot 02 outputs data from AD_OUT5 0101: Slot 02 outputs data from AD_OUT6 0110: Slot 02 outputs data from AD_OUT7 0111: Slot 02 outputs data from AD_OUT8 10xx: Slot 02 outputs zeros 11xx: Slot 02 is tristate

ADSlotSel3 — AD Data allocation in Slots 4 to 5

7	6	5	4	3	2	1	0
ADOToSlot5[3:0]				ADOToSlot4[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D21

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 4 to 5

[7:4]	**ADOToSlot5[3:0]** 0000: Slot 05 outputs data from AD_OUT1 0001: Slot 05 outputs data from AD_OUT2 0010: Slot 05 outputs data from AD_OUT3 0011: Slot 05 outputs data from AD_OUT4 0100: Slot 05 outputs data from AD_OUT5 0101: Slot 05 outputs data from AD_OUT6 0110: Slot 05 outputs data from AD_OUT7 0111: Slot 05 outputs data from AD_OUT8 10xx: Slot 05 outputs zeros 11xx: Slot 05 is tristate
[3:0]	**ADOToSlot4[3:0]** 0000: Slot 04 outputs data from AD_OUT1 0001: Slot 04 outputs data from AD_OUT2 0010: Slot 04 outputs data from AD_OUT3 0011: Slot 04 outputs data from AD_OUT4 0100: Slot 04 outputs data from AD_OUT5 0101: Slot 04 outputs data from AD_OUT6 0110: Slot 04 outputs data from AD_OUT7 0111: Slot 04 outputs data from AD_OUT8 10xx: Slot 04 outputs zeros 11xx: Slot 04 is tristate

ADSlotSel4 — AD Data allocation in Slots 6 to 7

7	6	5	4	3	2	1	0
ADOToSlot7[3:0]				ADOToSlot6[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D22

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 6 to 7

[7:4]	**ADOToSlot7[3:0]** 0000: Slot 07 outputs data from AD_OUT1 0001: Slot 07 outputs data from AD_OUT2 0010: Slot 07 outputs data from AD_OUT3 0011: Slot 07 outputs data from AD_OUT4 0100: Slot 07 outputs data from AD_OUT5 0101: Slot 07 outputs data from AD_OUT6 0110: Slot 07 outputs data from AD_OUT7 0111: Slot 07 outputs data from AD_OUT8 10xx: Slot 07 outputs zeros 11xx: Slot 07 is tristate
[3:0]	**ADOToSlot6[3:0]** 0000: Slot 06 outputs data from AD_OUT1 0001: Slot 06 outputs data from AD_OUT2 0010: Slot 06 outputs data from AD_OUT3 0011: Slot 06 outputs data from AD_OUT4 0100: Slot 06 outputs data from AD_OUT5 0101: Slot 06 outputs data from AD_OUT6 0110: Slot 06 outputs data from AD_OUT7 0111: Slot 06 outputs data from AD_OUT8 10xx: Slot 06 outputs zeros 11xx: Slot 06 is tristate

ADSlotSel5 — AD Data allocation in Slots 8 to 11

7	6	5	4	3	2	1	0
ADOToSlot9[3:0]				ADOToSlot8[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D23

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 8 to 9

[7:4]	**ADOToSlot9[3:0]** 0000: Slot 09 outputs data from AD_OUT1 0001: Slot 09 outputs data from AD_OUT2 0010: Slot 09 outputs data from AD_OUT3 0011: Slot 09 outputs data from AD_OUT4 0100: Slot 09 outputs data from AD_OUT5 0101: Slot 09 outputs data from AD_OUT6 0110: Slot 09 outputs data from AD_OUT7 0111: Slot 09 outputs data from AD_OUT8 10xx: Slot 09 outputs zeros 11xx: Slot 09 is tristate
[3:0]	**ADOToSlot8[3:0]** 0000: Slot 08 outputs data from AD_OUT1 0001: Slot 08 outputs data from AD_OUT2 0010: Slot 08 outputs data from AD_OUT3 0011: Slot 08 outputs data from AD_OUT4 0100: Slot 08 outputs data from AD_OUT5 0101: Slot 08 outputs data from AD_OUT6 0110: Slot 08 outputs data from AD_OUT7 0111: Slot 08 outputs data from AD_OUT8 10xx: Slot 08 outputs zeros 11xx: Slot 08 is tristate

ADSlotSel6 — AD Data allocation in Slots 10 to 11

7	6	5	4	3	2	1	0
ADOToSlot11[3:0]				ADOToSlot10[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D24

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 10 to 11

[7:4]	**ADOToSlot11[3:0]** 0000: Slot 11 outputs data from AD_OUT1 0001: Slot 11 outputs data from AD_OUT2 0010: Slot 11 outputs data from AD_OUT3 0011: Slot 11 outputs data from AD_OUT4 0100: Slot 11 outputs data from AD_OUT5 0101: Slot 11 outputs data from AD_OUT6 0110: Slot 11 outputs data from AD_OUT7 0111: Slot 11 outputs data from AD_OUT8 10xx: Slot 11 outputs zeros 11xx: Slot 11 is tristate
[3:0]	**ADOToSlot10[3:0]** 0000: Slot 10 outputs data from AD_OUT1 0001: Slot 10 outputs data from AD_OUT2 0010: Slot 10 outputs data from AD_OUT3 0011: Slot 10 outputs data from AD_OUT4 0100: Slot 10 outputs data from AD_OUT5 0101: Slot 10 outputs data from AD_OUT6 0110: Slot 10 outputs data from AD_OUT7 0111: Slot 10 outputs data from AD_OUT8 10xx: Slot 10 outputs zeros 11xx: Slot 10 is tristate

ADSlotSel7 — AD Data allocation in Slots 12 to 13

7	6	5	4	3	2	1	0
ADOToSlot13[3:0]				ADOToSlot12[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D25

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 12 to 13

[7:4]	**ADOToSlot13[3:0]** 0000: Slot 13 outputs data from AD_OUT1 0001: Slot 13 outputs data from AD_OUT2 0010: Slot 13 outputs data from AD_OUT3 0011: Slot 13 outputs data from AD_OUT4 0100: Slot 13 outputs data from AD_OUT5 0101: Slot 13 outputs data from AD_OUT6 0110: Slot 13 outputs data from AD_OUT7 0111: Slot 13 outputs data from AD_OUT8 10xx: Slot 13 outputs zeros 11xx: Slot 13 is tristate
[3:0]	**ADOToSlot12[3:0]** 0000: Slot 12 outputs data from AD_OUT1 0001: Slot 12 outputs data from AD_OUT2 0010: Slot 12 outputs data from AD_OUT3 0011: Slot 12 outputs data from AD_OUT4 0100: Slot 12 outputs data from AD_OUT5 0101: Slot 12 outputs data from AD_OUT6 0110: Slot 12 outputs data from AD_OUT7 0111: Slot 12 outputs data from AD_OUT8 10xx: Slot 12 outputs zeros 11xx: Slot 12 is tristate

ADSlotSel8 — AD Data allocation in Slots 14 to 15

7	6	5	4	3	2	1	0
ADOToSlot15[3:0]				ADOToSlot14[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D26

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 14 to 15

[7:4]	**ADOToSlot15[3:0]** 0000: Slot 15 outputs data from AD_OUT1 0001: Slot 15 outputs data from AD_OUT2 0010: Slot 15 outputs data from AD_OUT3 0011: Slot 15 outputs data from AD_OUT4 0100: Slot 15 outputs data from AD_OUT5 0101: Slot 15 outputs data from AD_OUT6 0110: Slot 15 outputs data from AD_OUT7 0111: Slot 15 outputs data from AD_OUT8 10xx: Slot 15 outputs zeros 11xx: Slot 15 is tristate
[3:0]	**ADOToSlot14[3:0]** 0000: Slot 14 outputs data from AD_OUT1 0001: Slot 14 outputs data from AD_OUT2 0010: Slot 14 outputs data from AD_OUT3 0011: Slot 14 outputs data from AD_OUT4 0100: Slot 14 outputs data from AD_OUT5 0101: Slot 14 outputs data from AD_OUT6 0110: Slot 14 outputs data from AD_OUT7 0111: Slot 14 outputs data from AD_OUT8 10xx: Slot 14 outputs zeros 11xx: Slot 14 is tristate

ADSlotSel9 — AD Data allocation in Slots 16 to 17

7	6	5	4	3	2	1	0
ADOToSlot17[3:0]				ADOToSlot16[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D27

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 16 to 17

[7:4]	**ADOToSlot17[3:0]** 0000: Slot 17 outputs data from AD_OUT1 0001: Slot 17 outputs data from AD_OUT2 0010: Slot 17 outputs data from AD_OUT3 0011: Slot 17 outputs data from AD_OUT4 0100: Slot 17 outputs data from AD_OUT5 0101: Slot 17 outputs data from AD_OUT6 0110: Slot 17 outputs data from AD_OUT7 0111: Slot 17 outputs data from AD_OUT8 10xx: Slot 17 outputs zeros 11xx: Slot 17 is tristate
[3:0]	**ADOToSlot16[3:0]** 0000: Slot 16 outputs data from AD_OUT1 0001: Slot 16 outputs data from AD_OUT2 0010: Slot 16 outputs data from AD_OUT3 0011: Slot 16 outputs data from AD_OUT4 0100: Slot 16 outputs data from AD_OUT5 0101: Slot 16 outputs data from AD_OUT6 0110: Slot 16 outputs data from AD_OUT7 0111: Slot 16 outputs data from AD_OUT8 10xx: Slot 16 outputs zeros 11xx: Slot 16 is tristate

ADSlotSel10 — AD Data allocation in Slots 18 to 19

7	6	5	4	3	2	1	0
ADOToSlot19[3:0]				ADOToSlot18[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D28

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 18 to 19

[7:4]	**ADOToSlot19[3:0]** 0000: Slot 19 outputs data from AD_OUT1 0001: Slot 19 outputs data from AD_OUT2 0010: Slot 19 outputs data from AD_OUT3 0011: Slot 19 outputs data from AD_OUT4 0100: Slot 19 outputs data from AD_OUT5 0101: Slot 19 outputs data from AD_OUT6 0110: Slot 19 outputs data from AD_OUT7 0111: Slot 19 outputs data from AD_OUT8 10xx: Slot 19 outputs zeros 11xx: Slot 19 is tristate
[3:0]	**ADOToSlot18[3:0]** 0000: Slot 18 outputs data from AD_OUT1 0001: Slot 18 outputs data from AD_OUT2 0010: Slot 18 outputs data from AD_OUT3 0011: Slot 18 outputs data from AD_OUT4 0100: Slot 18 outputs data from AD_OUT5 0101: Slot 18 outputs data from AD_OUT6 0110: Slot 18 outputs data from AD_OUT7 0111: Slot 18 outputs data from AD_OUT8 10xx: Slot 18 outputs zeros 11xx: Slot 18 is tristate

ADSlotSel11 — AD Data allocation in Slots 20 to 21

7	6	5	4	3	2	1	0
ADOToSlot21[3:0]				ADOToSlot20[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D29

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 20 to 21

[7:4]	**ADOToSlot21[3:0]** 0000: Slot 21 outputs data from AD_OUT1 0001: Slot 21 outputs data from AD_OUT2 0010: Slot 21 outputs data from AD_OUT3 0011: Slot 21 outputs data from AD_OUT4 0100: Slot 21 outputs data from AD_OUT5 0101: Slot 21 outputs data from AD_OUT6 0110: Slot 21 outputs data from AD_OUT7 0111: Slot 21 outputs data from AD_OUT8 10xx: Slot 21 outputs zeros 11xx: Slot 21 is tristate
[3:0]	**ADOToSlot20[3:0]** 0000: Slot 20 outputs data from AD_OUT1 0001: Slot 20 outputs data from AD_OUT2 0010: Slot 20 outputs data from AD_OUT3 0011: Slot 20 outputs data from AD_OUT4 0100: Slot 20 outputs data from AD_OUT5 0101: Slot 20 outputs data from AD_OUT6 0110: Slot 20 outputs data from AD_OUT7 0111: Slot 20 outputs data from AD_OUT8 10xx: Slot 20 outputs zeros 11xx: Slot 20 is tristate

ADSlotSel12 — AD Data allocation in Slots 22 to 23

7	6	5	4	3	2	1	0
ADOToSlot23[3:0]				ADOToSlot22[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D2A

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 22 to 23

[7:4]	**ADOToSlot23[3:0]** 0000: Slot 23 outputs data from AD_OUT1 0001: Slot 23 outputs data from AD_OUT2 0010: Slot 23 outputs data from AD_OUT3 0011: Slot 23 outputs data from AD_OUT4 0100: Slot 23 outputs data from AD_OUT5 0101: Slot 23 outputs data from AD_OUT6 0110: Slot 23 outputs data from AD_OUT7 0111: Slot 23 outputs data from AD_OUT8 10xx: Slot 23 outputs zeros 11xx: Slot 23 is tristate
[3:0]	**ADOToSlot22[3:0]** 0000: Slot 22 outputs data from AD_OUT1 0001: Slot 22 outputs data from AD_OUT2 0010: Slot 22 outputs data from AD_OUT3 0011: Slot 22 outputs data from AD_OUT4 0100: Slot 22 outputs data from AD_OUT5 0101: Slot 22 outputs data from AD_OUT6 0110: Slot 22 outputs data from AD_OUT7 0111: Slot 22 outputs data from AD_OUT8 10xx: Slot 22 outputs zeros 11xx: Slot 22 is tristate

ADSlotSel13 — AD Data allocation in Slots 24 to 25

7	6	5	4	3	2	1	0
ADOToSlot25[3:0]				ADOToSlot24[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D2B

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 24 to 25

[7:4]	**ADOToSlot25[3:0]** 0000: Slot 25 outputs data from AD_OUT1 0001: Slot 25 outputs data from AD_OUT2 0010: Slot 25 outputs data from AD_OUT3 0011: Slot 25 outputs data from AD_OUT4 0100: Slot 25 outputs data from AD_OUT5 0101: Slot 25 outputs data from AD_OUT6 0110: Slot 25 outputs data from AD_OUT7 0111: Slot 25 outputs data from AD_OUT8 10xx: Slot 25 outputs zeros 11xx: Slot 25 is tristate
[3:0]	**ADOToSlot24[3:0]** 0000: Slot 24 outputs data from AD_OUT1 0001: Slot 24 outputs data from AD_OUT2 0010: Slot 24 outputs data from AD_OUT3 0011: Slot 24 outputs data from AD_OUT4 0100: Slot 24 outputs data from AD_OUT5 0101: Slot 24 outputs data from AD_OUT6 0110: Slot 24 outputs data from AD_OUT7 0111: Slot 24 outputs data from AD_OUT8 10xx: Slot 24 outputs zeros 11xx: Slot 24 is tristate

ADSlotSel14 — AD Data allocation in Slots 26 to 27

7	6	5	4	3	2	1	0
ADOToSlot27[3:0]				ADOToSlot26[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D2C

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 26 to 27

[7:4]	**ADOToSlot27[3:0]** 0000: Slot 27 outputs data from AD_OUT1 0001: Slot 27 outputs data from AD_OUT2 0010: Slot 27 outputs data from AD_OUT3 0011: Slot 27 outputs data from AD_OUT4 0100: Slot 27 outputs data from AD_OUT5 0101: Slot 27 outputs data from AD_OUT6 0110: Slot 27 outputs data from AD_OUT7 0111: Slot 27 outputs data from AD_OUT8 10xx: Slot 27 outputs zeros 11xx: Slot 27 is tristate
[3:0]	**ADOToSlot26[3:0]** 0000: Slot 26 outputs data from AD_OUT1 0001: Slot 26 outputs data from AD_OUT2 0010: Slot 26 outputs data from AD_OUT3 0011: Slot 26 outputs data from AD_OUT4 0100: Slot 26 outputs data from AD_OUT5 0101: Slot 26 outputs data from AD_OUT6 0110: Slot 26 outputs data from AD_OUT7 0111: Slot 26 outputs data from AD_OUT8 10xx: Slot 26 outputs zeros 11xx: Slot 26 is tristate

ADSlotSel15 — AD Data allocation in Slots 28 to 29

7	6	5	4	3	2	1	0
ADOToSlot29[3:0]				ADOToSlot28[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D2D

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 28 to 29

[7:4]	**ADOToSlot29[3:0]** 0000: Slot 29 outputs data from AD_OUT1 0001: Slot 29 outputs data from AD_OUT2 0010: Slot 29 outputs data from AD_OUT3 0011: Slot 29 outputs data from AD_OUT4 0100: Slot 29 outputs data from AD_OUT5 0101: Slot 29 outputs data from AD_OUT6 0110: Slot 29 outputs data from AD_OUT7 0111: Slot 29 outputs data from AD_OUT8 10xx: Slot 29 outputs zeros 11xx: Slot 29 is tristate
[3:0]	**ADOToSlot28[3:0]** 0000: Slot 28 outputs data from AD_OUT1 0001: Slot 28 outputs data from AD_OUT2 0010: Slot 28 outputs data from AD_OUT3 0011: Slot 28 outputs data from AD_OUT4 0100: Slot 28 outputs data from AD_OUT5 0101: Slot 28 outputs data from AD_OUT6 0110: Slot 28 outputs data from AD_OUT7 0111: Slot 28 outputs data from AD_OUT8 10xx: Slot 28 outputs zeros 11xx: Slot 28 is tristate

ADSlotSel16 — AD Data allocation in Slots 30 to 31

7	6	5	4	3	2	1	0
ADOToSlot31[3:0]				ADOToSlot30[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D2E

Type: R/W

Reset: 0xCC

Description: AD data slot allocation for time slot from 30 to 31

[7:4]	**ADOToSlot31[3:0]** 0000: Slot 31 outputs data from AD_OUT1 0001: Slot 31 outputs data from AD_OUT2 0010: Slot 31 outputs data from AD_OUT3 0011: Slot 31 outputs data from AD_OUT4 0100:Slot 31 outputs data from AD_OUT5 0101: Slot 31 outputs data from AD_OUT6 0110: Slot 31 outputs data from AD_OUT7 0111: Slot 31 outputs data from AD_OUT8 10xx: Slot 31 outputs zeros 11xx: Slot 31 is tristate
[3:0]	**ADOToSlot30[3:0]** 0000: Slot 30 outputs data from AD_OUT1 0001: Slot 30 outputs data from AD_OUT2 0010: Slot 30 outputs data from AD_OUT3 0011: Slot 30 outputs data from AD_OUT4 0100: Slot 30 outputs data from AD_OUT5 0101: Slot 30 outputs data from AD_OUT6 0110: Slot 30 outputs data from AD_OUT7 0111: Slot 30 outputs data from AD_OUT8 10xx: Slot 30 outputs zeros 11xx: Slot 30 is tristate

ADSlotHizCtrl1 — AD slot 0/7 tristate

7	6	5	4	3	2	1	0
HizSlot7	HizSlot6	HizSlot5	HizSlot4	HizSlot3	HizSlot2	HizSlot1	HizSlot0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D2F

Type: R/W

Reset: 0x00

Description: AD slot 0/7 tristate control on last half MSB

[7]	**HizSlot7** 0: Slot 7 is in low impedance after last half-LSB (if not tristate) 1: Slot 7 is in high impedance after last half-LSB
[6]	**HizSlot6** 0: Slot 6 is in low impedance after last half-LSB (if not tristate) 1: Slot 6 is in high impedance after last half-LSB
[5]	**HizSlot5** 0: Slot 5 is in low impedance after last half-LSB (if not tristate) 1: Slot 5 is in high impedance after last half-LSB
[4]	**HizSlot4** 0: Slot 4 is in low impedance after last half-LSB (if not tristate) 1: Slot 4 is in high impedance after last half-LSB
[3]	**HizSlot3** 0: Slot 3 is in low impedance after last half-LSB (if not tristate) 1: Slot 3 is in high impedance after last half-LSB
[2]	**HizSlot2** 0: Slot 2 is in low impedance after last half-LSB (if not tristate) 1: Slot 2 is in high impedance after last half-LSB
[1]	**HizSlot1** 0: Slot 1 is in low impedance after last half-LSB (if not tristate) 1: Slot 1 is in high impedance after last half-LSB
[0]	**HizSlot0** 0: Slot 0 is in low impedance after last half-LSB (if not tristate) 1: Slot 0 is in high impedance after last half-LSB

ADSlotHizCtrl2 — AD slot 8/15 tristate

7	6	5	4	3	2	1	0
HizSlot15	HizSlot14	HizSlot13	HizSlot12	HizSlot11	HizSlot10	HizSlot9	HizSlot8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D30

Type: R/W

Reset: 0x00

Description: AD slot 8/15 tristate control on last half MSB

[7]	**HizSlot15** 0: Slot 15 is in low impedance after last half-LSB (if not tristate) 1: Slot 15 is in high impedance after last half-LSB
[6]	**HizSlot14** 0: Slot 14 is in low impedance after last half-LSB (if not tristate) 1: Slot 14 is in high impedance after last half-LSB
[5]	**HizSlot13** 0: Slot 13 is in low impedance after last half-LSB (if not tristate) 1: Slot 13 is in high impedance after last half-LSB
[4]	**HizSlot12** 0: Slot 12 is in low impedance after last half-LSB (if not tristate) 1: Slot 12 is in high impedance after last half-LSB
[3]	**HizSlot11** 0: Slot 11 is in low impedance after last half-LSB (if not tristate) 1: Slot 11 is in high impedance after last half-LSB
[2]	**HizSlot10** 0: Slot 10 is in low impedance after last half-LSB (if not tristate) 1: Slot 10 is in high impedance after last half-LSB
[1]	**HizSlot9** 0: Slot 9 is in low impedance after last half-LSB (if not tristate) 1: Slot 9 is in high impedance after last half-LSB
[0]	**HizSlot8** 0: Slot 8 is in low impedance after last half-LSB (if not tristate) 1: Slot 8 is in high impedance after last half-LSB

ADSlotHizCtrl3 — AD slot 16/23 tristate

7	6	5	4	3	2	1	0
HizSlot23	HizSlot22	HizSlot21	HizSlot20	HizSlot19	HizSlot18	HizSlot17	HizSlot16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D31

Type: R/W

Reset: 0x00

Description: AD slot 16/23 tristate control on last half MSB

[7]	**HizSlot23** 0: Slot 23 is in low impedance after last half-LSB (if not tristate) 1: Slot 23 is in high impedance after last half-LSB
[6]	**HizSlot22** 0: Slot 22 is in low impedance after last half-LSB (if not tristate) 1: Slot 22 is in high impedance after last half-LSB
[5]	**HizSlot21** 0: Slot 21 is in low impedance after last half-LSB (if not tristate) 1: Slot 21 is in high impedance after last half-LSB
[4]	**HizSlot20** 0: Slot 20 is in low impedance after last half-LSB (if not tristate) 1: Slot 20 is in high impedance after last half-LSB
[3]	**HizSlot19** 0: Slot 19 is in low impedance after last half-LSB (if not tristate) 1: Slot 19 is in high impedance after last half-LSB
[2]	**HizSlot18** 0: Slot 18 is in low impedance after last half-LSB (if not tristate) 1: Slot 18 is in high impedance after last half-LSB
[1]	**HizSlot17** 0: Slot 17 is in low impedance after last half-LSB (if not tristate) 1: Slot 17 is in high impedance after last half-LSB
[0]	**HizSlot16** 0: Slot 16 is in low impedance after last half-LSB (if not tristate) 1: Slot 16 is in high impedance after last half-LSB

ADSlotHizCtrl4 — AD slot 24/31 tristate

7	6	5	4	3	2	1	0
HizSlot31	HizSlot30	HizSlot29	HizSlot28	HizSlot27	HizSlot26	HizSlot25	HizSlot24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D32

Type: R/W

Reset: 0x00

Description: AD slot 24/31 tristate control on last half MSB

[7]	**HizSlot31** 0: Slot 31 is in low impedance after last half-LSB (if not tristate) 1: Slot 31 is in high impedance after last half-LSB
[6]	**HizSlot30** 0: Slot 30 is in low impedance after last half-LSB (if not tristate) 1: Slot 30 is in high impedance after last half-LSB
[5]	**HizSlot29** 0: Slot 29 is in low impedance after last half-LSB (if not tristate) 1: Slot 29 is in high impedance after last half-LSB
[4]	**HizSlot28** 0: Slot 28 is in low impedance after last half-LSB (if not tristate) 1: Slot 28 is in high impedance after last half-LSB
[3]	**HizSlot27** 0: Slot 27 is in low impedance after last half-LSB (if not tristate) 1: Slot 27 is in high impedance after last half-LSB
[2]	**HizSlot26** 0: Slot 26 is in low impedance after last half-LSB (if not tristate) 1: Slot 26 is in high impedance after last half-LSB
[1]	**HizSlot25** 0: Slot 25 is in low impedance after last half-LSB (if not tristate) 1: Slot 25 is in high impedance after last half-LSB
[0]	**HizSlot24** 0: Slot 24 is in low impedance after last half-LSB (if not tristate) 1: Slot 24 is in high impedance after last half-LSB

DA channels allocation from TDM Audio Interface slots

DASlotConf1 — Slots selection for DA path 1

7	6	5	4	3	2	1	0
DA12Voice	SwapDA12_34	DAI7ToADO1	SLToDA1[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D33

Type: R/W

Reset: 0x08

Description: Slot selection for DA path 1

[7]	**DA12Voice** 0: DA1 and DA2 channel paths use Audio Filters 1: DA1 and DA2 channel paths use 48 kHz Low Latency Filters for Voice
[6]	**SwapDA12_34** 0: Normal operation 1: DA channels 1 and 2 are swapped with DA channels 3 and 4 before channel filtering
[5]	**DAI7ToADO1** 0: AD_OUT1 is connected to the corresponding AD path 1: DA_IN7 is looped back to AD_OUT1
[4:0]	**SLToDA1[4:0]** Data sent to DA1 input of DA filter (DSP) 00000: Slot 00 (AUD_IF0, AD_Data0) 00001: Slot 01 (AUD_IF0, AD_Data0) 00xxx: Slot 02-07 (AUD_IF0, AD_Data0) 01000: Slot 08 (AUD_IF0, DA_Data0) 01001: Slot 09 (AUD_IF0, DA_Data0) 01xxx: Slot 10 to15 (AUD_IF0, DA_Data0) 10000: Slot 16 (AUD_IF1, AD_Data0) 10001: Slot 17 (AUD_IF1, AD_Data0) 10xxx: Slot 18 to 23 (AUD_IF1, AD_Data0) 11000: Slot 24 (AUD_IF1, DA_Data0) 11001: Slot 25 (AUD_IF1, DA_Data0) 11xxx: Slot 26 to 31 (AUD_IF1, DA_Data0)

DASlotConf2 — Slots selection for DA path 2

7	6	5	4	3	2	1	0
Reserved		DAI8ToADO2	SLToDA2[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D34

Type: R/W

Reset: 0x08

Description: Slot selection for DA path 2

[7:6]	Reserved
[5]	**DAI8ToADO2** 0: AD_OUT2 is connected to the corresponding AD path 1: DA_IN8 is looped back to AD_OUT2
[4:0]	**SLToDA2[4:0]** Data sent to DA2 input of DA filter (DSP) 00000: Slot 00 (AUD_IF0, AD_Data0) 00001 to 01110: Slot 01 to Slot 14(AUD_IF0, AD_Data0) 01111: Slot 15 (AUD_IF0, DA_Data0) 10000: Slot 16 (AUD_IF1, AD_Data0) 10001 to 11110: Slot 17 to Slot 30 (AUD_IF1, AD_Data0) 11111: Slot 31 (AUD_IF1, DA_Data0)

DASlotConf3 — Slots selection for DA path 3

7	6	5	4	3	2	1	0
DA34Voice	Reserved	DAI7ToADO3	SLToDA3[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D35

Type: R/W

Reset: 0x08

Description: Slot selection for DA path 3

[7]	**DA34Voice** 0: DA3 and DA4 channel paths use Audio Filters 1: DA3 and DA4 channel paths use 48 kHz Low Latency Filters for Voice
[6]	Reserved
[5]	**DAI7ToADO3** 0: AD_OUT3 is connected to the corresponding AD path 1: DA_IN7 is looped back to AD_OUT3
[4:0]	**SLToDA3[4:0]** Data sent to DA3 input of DA filter (DSP) 00000: Slot 00 (AUD_IF0, AD_Data0) 00001 to 01110: Slot 01 to Slot 14(AUD_IF0, AD_Data0) 01111: Slot 15 (AUD_IF0, DA_Data0) 10000: Slot 16 (AUD_IF1, AD_Data0) 10001 to 11110: Slot 17 to Slot 30 (AUD_IF1, AD_Data0) 11111: Slot 31 (AUD_IF1, DA_Data0)

DASlotConf4 — Slots selection for DA path 4

7	6	5	4	3	2	1	0
Reserved		DAI8ToADO4	SLToDA4[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D36

Type: R/W

Reset: 0x08

Description: Slot selection for DA path 4

[7:6]	Reserved
[5]	**DAI8ToADO4** 0: AD_OUT4 is connected to the corresponding AD path 1: DA_IN8 is looped back to AD_OUT4
[4:0]	**SLToDA4[4:0]** Data sent to DA4 input of DA filter (DSP) 00000: Slot 00 (AUD_IF0, AD_Data0) 00001 to 01110: Slot 01 to Slot 14(AUD_IF0, AD_Data0) 01111: Slot 15 (AUD_IF0, DA_Data0) 10000: Slot 16 (AUD_IF1, AD_Data0) 10001 to 11110: Slot 17 to Slot 30 (AUD_IF1, AD_Data0) 11111: Slot 31 (AUD_IF1, DA_Data0)

DASlotConf5 — Slots selection for DA path 5

7	6	5	4	3	2	1	0
DA56Voice	Reserved	DAI7ToADO5	SLToDA5[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D37

Type: R/W

Reset: 0x08

Description: Slot selection for DA path 5

[7]	**DA56Voice** 0: DA5 and DA6 channel paths use Audio Filters 1: DA5 and DA6 channel paths use 48 kHz Low Latency Filters for Voice
[6]	Reserved
[5]	**DAI7ToADO5** 0: AD_OUT5 is connected to the corresponding AD path 1: DA_IN7 is looped back to AD_OUT5
[4:0]	**SLToDA5[4:0]** Data sent to DA5 input of DA filter (DSP) 00000: Slot 00 (AUD_IF0, AD_Data0) 00001 to 01110: Slot 01 to Slot 14(AUD_IF0, AD_Data0) 01111: Slot 15 (AUD_IF0, DA_Data0) 10000: Slot 16 (AUD_IF1, AD_Data0) 10001 to 11110: Slot 17 to Slot 30 (AUD_IF1, AD_Data0) 11111: Slot 31 (AUD_IF1, DA_Data0)

DASlotConf6 — Slots selection for DA path 6

7	6	5	4	3	2	1	0
Reserved		DAI8ToADO6	SLToDA6[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D38

Type: R/W

Reset: 0x08

Description: Slot selection for DA path 6

[7:6]	Reserved
[5]	**DAI8ToADO6** 0: AD_OUT6 is connected to the corresponding AD path 1: DA_IN8 is looped back to AD_OUT6
[4:0]	**SLToDA6[4:0]** Data sent to DA6 input of DA filter (DSP) 00000: Slot 00 (AUD_IF0, AD_Data0) 00001 to 01110: Slot 01 to Slot 14(AUD_IF0, AD_Data0) 01111: Slot 15 (AUD_IF0, DA_Data0) 10000: Slot 16 (AUD_IF1, AD_Data0) 10001 to 11110: Slot 17 to Slot 30 (AUD_IF1, AD_Data0) 11111: Slot 31 (AUD_IF1, DA_Data0)

DASlotConf7 — Slots selection for DA path 7

7	6	5	4	3	2	1	0
Reserved		DAI8ToADO7	SLToDA7[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D39

Type: R/W

Reset: 0x08

Description: Slot selection for DA path 7

[7:6]	Reserved
[5]	**DAI8ToADO7** 0: AD_OUT7 is connected to the corresponding AD path 1: DA_IN8 is looped back to AD_OUT7
[4:0]	**SLToDA7[4:0]** Data sent to DA7 input of DA filter (DSP) 00000: Slot 00 (AUD_IF0, AD_Data0) 00001 to 01110: Slot 01 to Slot 14(AUD_IF0, AD_Data0) 01111: Slot 15 (AUD_IF0, DA_Data0) 10000: Slot 16 (AUD_IF1, AD_Data0) 10001 to 11110: Slot 17 to Slot 30 (AUD_IF1, AD_Data0) 11111: Slot 31 (AUD_IF1, DA_Data0)

DASlotConf8 — Slots selection for DA path 8

7	6	5	4	3	2	1	0
Reserved		DAI7ToADO8	SLToDA8[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D3A

Type: R/W

Reset: 0x08

Description: Slot selection for DA path 6

[7:6]	Reserved
[5]	**DAI8ToADO6** 0: AD_OUT8 is connected to the corresponding AD path 1: DA_IN7 is looped back to AD_OUT8
[4:0]	**SLToDA8[4:0]** Data sent to DA8 input of DA filter (DSP) 00000: Slot 00 (AUD_IF0, AD_Data0) 00001 to 01110: Slot 01 to Slot 14(AUD_IF0, AD_Data0) 01111: Slot 15 (AUD_IF0, DA_Data0) 10000: Slot 16 (AUD_IF1, AD_Data0) 10001 to 11110: Slot 17 to Slot 30 (AUD_IF1, AD_Data0) 11111: Slot 31 (AUD_IF1, DA_Data0)

Class-D EMI Control

ClassDConf1 — Class-D EMI Control

7	6	5	4	3	2	1	0
ParlHf	ParlVib	Reserved		ClassDVib1 SwapEn	ClassDVib2 SwapEn	ClassDHfL SwapEn	ClassDHfR SwapEn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D3B

Type: R/W

Reset: 0x00

Description: Class-D EMI controls enables.

[7]	**ParlHf**[1] 0: The HfL and HfR Outputs are independent 1: The HfL and HfR Outputs are connected in parallel. HfL path is used for both
[6]	**ParlVib** 0: The Vib1 and Vib2 Outputs are independent 1: The Vib1 and Vib2 Outputs are connected in parallel. Vib1 path is used for both
[5:4]	Reserved
[3]	**ClassDVib1SwapEn** 0: Low EMI mode for Vib1 disabled. 1: Low EMI mode for Vib1 enabled.
[2]	**ClassDVib2SwapEn** 0: Low EMI mode for Vib2 disabled. 1: Low EMI mode for Vib2 enabled.
[1]	**ClassDHfLSwapEn** 0: Low EMI mode for HfL disabled. 1: Low EMI mode for HfL enabled.
[0]	**ClassDHfRSwapEn** 0: Low EMI mode for HfR disabled. 1: Low EMI mode for HfR enabled.

1. Both L and R drivers must be enabled to have the parallel mode.

ClassDConf2 — Class-D control path

7	6	5	4	3	2	1	0
ClassDFIRByp[3:0]				ClassDHighVolEn[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D3C

Type: R/W

Reset: 0x00

Description: Class-D path control.

[7:4]	**ClassDFIRByp[3:0]** 0000: All Pwm FIRs are enabled xxx1: Left Hf Pwm FIR filter is bypassed xx1x: Right Hf Pwm FIR filter is bypassed x1xx: Vibra1 Pwm FIR filter is bypassed 1xxx: Vibra2 Pwm FIR filter is bypassed
[3:0]	**ClassDHighVolEn[3:0]** 0000: High volume mode disabled xxx1: Left Hf channel in high volume mode (+2 dB) xx1x: Right Hf channel in high volume mode (+2 dB) x1xx: Vibra1 channel in high volume mode (+2 dB) 1xxx: Vibra2 channel in high volume mode (+2 dB) *Note: These register bits cannot be changed on the fly if 'EnHfL' or 'EnHfR' or 'EnVib1' or 'EnVib2' bit, is set to "1" (AnaConf4 register)*

ClassDConf3 — Class-D control gain

7	6	5	4	3	2	1	0
ClassDDithHPGain[3:0]				ClassDDithWGain[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D3D

Type: R/W

Reset: 0x84

Description: Class-D dithering control.

[7:4]	**ClassDDithHPGain[3:0]** Gain control for the high pass component of dithering filter 0000: Minimum gain .....: 1010: Maximum gain
[3:0]	**ClassDDithWGain[3:0]** Gain control for the white component of dithering filter 0000: Minimum gain .....: 1010: Maximum gain

Dmic decimator filter

DmicFiltConf — Dmic decimation filter

7	6	5	4	3	2	1	0
ANCInSel	DA3ToEar	Dmic1Sinc3	Dmic2Sinc3	Dmic3Sinc3	Dmic4Sinc3	Dmic5Sinc3	Dmic6Sinc3
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0D3E

Type: R/W

Reset: 0x00

Description: Dmic Decimator filter Sinc orders

[7]	**ANCInSel** 0: ANC input is AD6 path 1: ANC input is AD5 path
[6]	**DA3ToEar** 0: EarDAC signal comes from DA1 path 1: EarDAC signal comes from DA3 path
[5]	**Dmic1Sinc3** 0: Sinc5 decimator filter is selected for Dmic1 1: Sinc3 decimator filter is selected for Dmic1
[4]	**Dmic2Sinc3** 0: Sinc5 decimator filter is selected for Dmic2 1: Sinc3 decimator filter is selected for Dmic2
[3]	**Dmic3Sinc3** 0: Sinc5 decimator filter is selected for Dmic3 1: Sinc3 decimator filter is selected for Dmic3
[2]	**Dmic4Sinc3** 0: Sinc5 decimator filter is selected for Dmic4 1: Sinc3 decimator filter is selected for Dmic4
[1]	**Dmic5Sinc3** 0: Sinc5 decimator filter is selected for Dmic5 1: Sinc3 decimator filter is selected for Dmic5
[0]	**Dmic6Sinc3** 0: Sinc5 decimator filter is selected for Dmic6 1: Sinc3 decimator filter is selected for Dmic6

Digital Multiplexers configuration

DigMultConf1 — Multiplexers LSB

7	6	5	4	3	2	1	0
DAToHsLEn	DAToHsREn	AD1Sel	AD2Sel	AD3Sel	AD5Sel	AD6Sel	ANCSel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D3F

Type: R/W

Reset: 0xFE

Description: Multiplexers LSB register features

[7]	**DAToHsLEn** 0: DA_IN1 direct path disabled. Path from sidetone FIR connected to HsL. 1: DA_IN1 path mixed together with sidetone FIR.
[6]	**DAToHsREn** 0: DA_IN2 direct path disabled. Path from sidetone FIR connected to HsR. 1: DA_IN2 path mixed together with sidetone FIR.
[5]	**AD1Sel** 0:Left Linein ADC1LinL analog input is selected for AD_OUT1 output path 1: Digital microphone Dmic1 is selected for AD_OUT1 output path
[4]	**AD2Sel** 0:Right Linein ADC2linR analog input is selected for AD_OUT2 output path 1: Digital microphone Dmic2 is selected for AD_OUT2 output path
[3]	**AD3Sel** 0:Analog microphone ADC3Mic analog input is selected for AD_OUT3 output path 1: Digital microphone Dmic3 is selected for AD_OUT3 output path
[2]	**AD5Sel** 0:Analog microphone on ADC2LinR analog input is selected for AD_OUT5 output path 1: Digital microphone Dmic5 is selected for AD_OUT5 output path
[1]	**AD6Sel** 0:Analog microphone on ADC3Mic analog input is selected for AD_OUT6/ANC output path 1: Digital microphone Dmic6 is selected for AD_OUT6/ANC output path
[0]	**ANCSel** 0: ANC loop not mixed in earpiece driver. 1: ANC loop mixed in earpiece driver.

DigMultConf2 — Multiplexers msb

7	6	5	4	3	2	1	0
DATtoHfREn	DATtoHfLEn	HfRSel	HfLSel	FIRSid1Sel[1:0]		FIRSid2Sel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D40

Type: R/W

Reset: 0xC0

Description: Digital multiplexers(1)

[7]	**DAToHfREn** 0: DA4 or ANC path to HfR is muted 1: DA4 or ANC path to HfR is enabled
[6]	**DAToHfLEn** 0: DA3 or ANC path to HfL is muted 1: DA3 or ANC path to HfL is enabled
[5]	**HfRSel** 0: HfR data comes from DA4 if ‘DAToHfREn’=1 1: HfR data comes from ANC if ‘DAToHfREn’=1
[4]	**HfLSel** 0: HfL data comes from DA3 if ‘DAToHfLEn’=1 1: HfL data comes from ANC if ‘DAToHfLEn’=1
[3:2]	**FIRSid1Sel[1:0]** 00: FIR1 data comes from AD_OUT1 01: FIR1 data comes from AD_OUT2 10: FIR1 data comes from AD_OUT3 11: FIR1 data comes from DA_IN1
[1:0]	**FIRSid2Sel[1:0]** 00: FIR2 data comes from AD_OUT2 01: FIR2 data comes from AD_OUT3 10: FIR2 data comes from AD_OUT4 11: FIR2 data comes from DA_IN2

(1) see *Figure 35: Digital AD and DA paths block Registers*

AD paths digital gains

ADDigGain1 — AD1 Digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisAD1	AD1Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D41

Type: R/W

Reset: 0x3F

Description: AD1 path digital gain

[7]	Reserved
[6]	**FadeDisAD1** 0: Fading (anti-click) on AD1 path is active 1: Fading (anti-click) on AD1 path is disabled
[5:0]	**AD1Gain[5:0]** AD1 path digital gain 000000: 31 dB gain 000001: 30 dB gain .....: 1 dB step 011111: 0 dB gain .....: 1 dB step 111101: -30 dB gain 111110: -31 dB gain 111111: -inf dB gain (mute)

ADDigGain2 AD2 Digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisAD2	AD2Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D42

Type: R/W

Reset: 0x3F

Description: AD2 path digital gain

[7]	Reserved
[6]	**FadeDisAD2** 0: Fading (anti-click) on AD2 path is active 1: Fading (anti-click) on AD2 path is disabled
[5:0]	**AD2Gain[5:0]** AD2 path digital gain 000000: 31 dB gain 000001: 30 dB gain .....: 1 dB step 011111: 0 dB gain .....: 1 dB step 111101: -30 dB gain 111110: -31 dB gain 111111: -inf dB gain (mute)

ADDigGain3 — AD3 Digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisAD3	AD3Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D43

Type: R/W

Reset: 0x3F

Description: AD3 path digital gain

[7]	Reserved
[6]	**FadeDisAD3** 0: Fading (anti-click) on AD3 path is active 1: Fading (anti-click) on AD3 path is disabled
[5:0]	**AD3Gain[5:0]** AD3 path digital gain 000000: 31 dB gain 000001: 30 dB gain .....: 1 dB step 011111: 0 dB gain .....: 1 dB step 111101: -30 dB gain 111110: -31 dB gain 111111: -inf dB gain (mute)

ADDigGain4 AD4 Digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisAD4	AD4Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D44

Type: R/W

Reset: 0x3F

Description: AD4 path digital gain

[7]	Reserved
[6]	**FadeDisAD4** 0: Fading (anti-click) on AD4 path is active 1: Fading (anti-click) on AD4 path is disabled
[5:0]	**AD4Gain[5:0]** AD4 path digital gain 000000: 31 dB gain 000001: 30 dB gain .....: 1 dB step 011111: 0 dB gain .....: 1 dB step 111101: -30 dB gain 111110: -31 dB gain 111111: -inf dB gain (mute)

ADDigGain5 AD5 Digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisAD5	AD5Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D45

Type: R/W

Reset: 0x3F

Description: AD5 path digital gain

[7]	Reserved
[6]	**FadeDisAD5** 0: Fading (anti-click) on AD5 path is active 1: Fading (anti-click) on AD5 path is disabled
[5:0]	**AD5Gain[5:0]** AD5 path digital gain 000000: 31 dB gain 000001: 30 dB gain .....: 1 dB step 011111: 0 dB gain .....: 1 dB step 111101: -30 dB gain 111110: -31 dB gain 111111: -inf dB gain (mute)

ADDigGain6 AD6 Digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisAD6	AD6Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D46

Type: R/W

Reset: 0x3F

Description: AD6 path digital gain

[7]	Reserved
[6]	**FadeDisAD6** 0: Fading (anti-click) on AD6 path is active 1: Fading (anti-click) on AD6 path is disabled
[5:0]	**AD6Gain[5:0]** AD6 path digital gain 000000: 31 dB gain 000001: 30 dB gain .....: 1 dB step 011111: 0 dB gain .....: 1 dB step 111101: -30 dB gain 111110: -31 dB gain 111111: -inf dB gain (mute)

DA paths digital gains

DADigGain1 — DA1 Digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisDA1	DA1Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D47

Type: R/W

Reset: 0x3F

Description: DA1 path digital gain

[7]	Reserved
[6]	**FadeDisDA1** 0: Fading (anti-click) on DA1 path is active 1: Fading (anti-click) on DA1 path is disabled
[5:0]	**DA1Gain[5:0]** DA1 path digital gain 000000: 0 dB gain 000001: -1 dB gain .....: -1 dB step 011111: -31 dB gain .....: -1 dB step 111101: -61 dB gain 111110: -62 dB gain 111111: -inf dB gain (mute)

DADigGain2 DA2 Digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisDA2	DA2Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D48

Type: R/W

Reset: 0x3F

Description: DA2 path digital gain

[7]	Reserved
[6]	**FadeDisDA2** 0: Fading (anti-click) on DA2 path is active 1: Fading (anti-click) on DA2 path is disabled
[5:0]	**DA2Gain[5:0]** DA1 path digital gain 000000: 0 dB gain 000001: -1 dB gain .....: -1 dB step 011111: -31 dB gain .....: -1 dB step 111101: -61 dB gain 111110: -62 dB gain 111111: -inf dB gain (mute)

DADigGain3 — DA3 Digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisDA3	DA3Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D49

Type: R/W

Reset: 0x3F

Description: DA3 path digital gain

[7]	Reserved
[6]	**FadeDisDA3** 0: Fading (anti-click) on DA3 path is active 1: Fading (anti-click) on DA3 path is disabled
[5:0]	**DA3Gain[5:0]** DA3 path digital gain 000000: 0 dB gain 000001: -1 dB gain .....: -1 dB step 011111: -31 dB gain .....: -1 dB step 111101: -61 dB gain 111110: -62 dB gain 111111: -inf dB gain (mute)

DADigGain4 DA4 Digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisDA4	DA4Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D4A

Type: R/W

Reset: 0x3F

Description: DA4 path digital gain

[7]	Reserved
[6]	**FadeDisDA4** 0: Fading (anti-click) on DA4 path is active 1: Fading (anti-click) on DA4 path is disabled
[5:0]	**DA4Gain[5:0]** DA4 path digital gain 000000: 0 dB gain 000001: -1 dB gain .....: -1 dB step 011111: -31 dB gain .....: -1 dB step 111101: -61 dB gain 111110: -62 dB gain 111111: -inf dB gain (mute)

DADigGain5 — DA5 digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisDA5	DA5Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D4B

Type: R/W

Reset: 0x3F

Description: DA5 path digital gain

[7]	Reserved
[6]	**FadeDisDA5** 0: Fading (anti-click) on DA5 path is active 1: Fading (anti-click) on DA5 path is disabled
[5:0]	**DA5Gain[5:0]** DA5 path digital gain 000000: 0 dB gain 000001: -1 dB gain .....: -1 dB step 011111: -31 dB gain .....: -1 dB step 111101: -61 dB gain 111110: -62 dB gain 111111: -inf dB gain (mute)

DADigGain6 — DA6 digital Gain

7	6	5	4	3	2	1	0
Reserved	FadeDisDA6	DA6Gain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D4C

Type: R/W

Reset: 0x3F

Description: DA6 path digital gain

[7]	Reserved
[6]	**FadeDisDA6** 0: Fading (anti-click) on DA6 path is active 1: Fading (anti-click) on DA6 path is disabled
[5:0]	**DA6Gain[5:0]** DA6 path digital gain 000000: 0 dB gain 000001: -1 dB gain .....: -1 dB step 011111: -31 dB gain .....: -1 dB step 111101: -61 dB gain 111110: -62 dB gain 111111: -inf dB gain (mute)

Loopbacks digital gains

ADDigLoopGain1 — AD1 loopback to HfL digital gain

7	6	5	4	3	2	1	0
Reserved	FadeDisAD1L	AD1LBGain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D4D

Type: R/W

Reset: 0x3F

Description: AD1 path digital gain on loop to Left Hand free driver

[7]	Reserved
[6]	**FadeDisAD1L** 0: Fading (anti-click) on AD1 loop to HfL is active 1: Fading (anti-click) on AD1 loop to HfL is disabled
[5:0]	**AD1LBGain[5:0]** AD1 path digital gain on loop to HfL 000000: 0 dB gain 000001: -1 dB gain .....: -1 dB step 011111: -31 dB gain .....: -1 dB step 111101: -61 dB gain 111110: -62 dB gain 111111: -inf dB gain (mute)

ADDigLoopGain2 — AD2 loopback to HfR digital gain

7	6	5	4	3	2	1	0
Reserved	FadeDisAD2L	AD2LBGain[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D4E

Type: R/W

Reset: 0x3F

Description: AD2 path digital gain on loop to Right Hand free driver

[7]	Reserved
[6]	**FadeDisAD2L** 0: Fading (anti-click) on AD2 loop to HfR is active 1: Fading (anti-click) on AD2 loop to HfR is disabled
[5:0]	**AD2LBGain[5:0]** AD2 path digital gain on loop to HfR 000000: 0 dB gain 000001: -1 dB gain .....: -1 dB step 011111: -31 dB gain .....: -1 dB step 111101: -61 dB gain 111110: -62 dB gain 111111: -inf dB gain (mute)

Output drivers digital gains

HsLEarDigGain — HsL/Ear digital gain

7	6	5	4	3	2	1	0
HsSinc1	Reserved		FadeDisHsL	HsLDGain[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D4F

Type: R/W

Reset: 0x0F

Description: HsL/Earpiece digital gain

[7]	**HsSinc1** 0: sinc3 interpolator chosen for Hs or Earpiece drivers 1: sinc1 (hold) interpolator chosen for Hs or Earpiece drivers *Note: this bit cannot be changed on the fly with the digital channel enabled (if 'EnDACEar' or 'EnDACHsL' or 'EnDacHsR' bit (DAPathConf register) is set to "1")*
[6:5]	Reserved
[4]	**FadeDisHsL** 0: Fading (anti-click) on HsL digital gain is active 1: Fading (anti-click) on HsL digital gain is disabled
[3:0]	**HsLDGain[3:0]** HsL or Earpiece path digital gain 0000: +8 dB gain 0001: +7 dB gain .....: -1 dB step 0111: +1 dB gain 1000: 0 dB gain 1001 to 1111: -inf dB gain (mute)

HsRDigGain — HsR digital gain

7	6	5	4	3	2	1	0
FadeSpeed[1:0]		Reserved	FadeDisHsR	HsRDGain[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D50

Type: R/W

Reset: 0x0F

Description: HsR digital gain

[7:6]	**FadeSpeed[1:0]** Approximate time between each 1 dB step digital gain change 00: 1 ms 01: 4 ms 10: 8 ms 11: 16 ms The fade speed applies to digital gains g1, g2 and g4. (see *Figure 35*) The automatic fading can be individually disabled with 'FadeDis(xxx)' bits
[5]	Reserved
[4]	**FadeDisHsR** 0: Fading (anti-click) on HsR digital gain is active 1: Fading (anti-click) on HsR digital gain is disabled
[3:0]	**HsRDGain[3:0]** HsR path digital gain 0000: +8 dB gain 0001: +7 dB gain .....: -1 dB step 0111: +1 dB gain 1000: 0 dB gain 1001 to 1111: -inf dB gain (mute)

Side tone FIRs gain

SidFIRGain1 — Side tone FIR1 gain

7	6	5	4	3	2	1	0
Reserved			FIRSid1Gain[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D51

Type: R/W

Reset: 0x1F

Description: Digital gain for sidetone FIR1 path

[7:5]	Reserved
[4:0]	**FIRSid1Gain[4:0]** Digital gain for side tone 1 path. 00000: 0 dB gain 00001: -1 dB gain .....: -1 dB step 11101: -29 dB gain 11110: -30 dB gain 11111: -inf dB gain (mute)

SidFIRGain2 — Side tone FIR2 gain

7	6	5	4	3	2	1	0
Reserved			FIRSid2Gain[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D52

Type: R/W

Reset: 0x1F

Description: Digital gain for sidetone FIR2 path

[7:5]	Reserved
[4:0]	**FIRSid2Gain[4:0]** Digital gain for side tone 2 path. 00000: 0 dB gain 00001: -1 dB gain .....: -1 dB step 11101: -29 dB gain 11110: -30 dB gain 11111: -inf dB gain (mute)

Acoustical Noise Cancellation (ANC) Control

ANCConf1 — ANC filter control

7	6	5	4	3	2	1	0
Reserved				ANCIIRUpdate	EnANC	ANCIIRInit	ANCFIRUpdate
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D53

Type: R/W

Reset: 0x00

Description: ANC digital gain for Warped Delay Line input

[7:4]	Reserved
[3]	**ANCIIRUpdate** 0: ANC IIR coefficient pointer is reset (unless 'ANCIIRInit' bit is used). 1: ANC IIR coefficient pointer is removed from reset and IIR coefficients can be updated.
[2]	**EnANC** 0: ANC functions are disabled. FIR and IIR coefficients cannot be accessed for writing. 1: ANC functions are enabled.
[1]	**ANCIIRInit** 0: IIR initialization cannot start 1: Indicate the start of IIR initialization. IIR coefficients can be written for the first time.
[0]	**ANCFIRUpdate** 0: ANC FIR coefficient pointer is reset. 1: ANC FIR coefficient pointer is removed from reset and IIR coefficients can be updated.

ANCConf2 — ANC Warped Delay Line Shift

7	6	5	4	3	2	1	0
Reserved			ANCInShift[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D54

Type: R/W

Reset: 0x00

Description: ANC digital gain for Warped Delay Line input

[7:5]	Reserved
[4:0]	**ANCInShift[4:0]** Digital gain for Warped Delay Line input. 01111: Shift left by 15 steps 01110: Shift left by 14 steps .....: 00001: Shift left by 1 step 00000: Does not shift 11111: Shift right by 1 steps .....: 10000: Shift right by 16 steps

ANCConf3 ANC FIR output Shift

7	6	5	4	3	2	1	0
Reserved			ANCFIROutShift[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D55

Type: R/W

Reset: 0x00

Description: ANC digital gain for FIR output

[7:5]	Reserved
[4:0]	**ANCFIROutShift[4:0]** Digital gain for FIR output filter. 01111: Shift left by 15 steps 01110: Shift left by 14 steps .....: 00001: Shift left by 1 step 00000: Does not shift 11111: Shift right by 1 steps .....: 10000: Shift right by 16 steps

ANCConf4 ANC IIR output Shift

7	6	5	4	3	2	1	0
Reserved			ANCShiftOut[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D56

Type: R/W

Reset: 0x00

Description: ANC digital gain for IIR output

[7:5]	Reserved
[4:0]	**ANCShiftOut[4:0]** Digital gain for IIR output filter. 01111: Shift left by 15 steps 01110: Shift left by 14 steps .....: 00001: Shift left by 1 step 00000: Does not shift 11111: Shift right by 1 steps .....: 10000:Shift right by 16 steps

ANCConf5 ANC FIR coefficients msb

7	6	5	4	3	2	1	0
ANCFIRCoeffMSB[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D57

Type: R/W

Reset: 0x00

Description: ANC FIR filter coefficient MSB part.

[7:0]	**ANCFIRCoeffMSB[7:0]** Sets the MSB of the ANC FIR coefficients, the 16 bits coefficient is updated when the LSB part is written. See ANCFIRCoeffLSB[7:0] for details

ANCConf6 ANC FIR coefficients lsb

7	6	5	4	3	2	1	0
ANCFIRCoeffLSB[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D58

Type: R/W

Reset: 0x00

Description: ANC FIR filter coefficient LSB part.

[7:0]	**ANCFIRCoeffLSB[7:0]** Sets the LSB of the ANC FIR coefficients, it updates the 16 bits coefficient and it increases the coefficient pointer. The FIR coefficients are 15 and they are written sequentially from 0 to 14. The coefficient bank must be written setting first ‘ANCFIRUpDate’=1 and it is applied when the last coefficient is written. When ‘ANCFIRUpDate’ is set to zero the coefficient pointer is reset.

ANCConf7 ANC IIR coefficients MSB

7	6	5	4	3	2	1	0
ANCIIRCoeffMSB[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D59

Type: R/W

Reset: 0x00

Description: ANC IIR filter coefficient MSB part.

[7:0]	**ANCIIRCoeffMSB[7:0]** Sets the MSB of the ANC IIR coefficients, the 16 bits coefficient is updated when the LSB part is written. See ANCIIRCoeffLSB for details.

ANCConf8 ANC IIR coefficients LSB

7	6	5	4	3	2	1	0
ANCIIRCoeffLSB[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D5A

Type: R/W

Reset: 0x00

Description: ANC IIR filter coefficient LSB part

[7:0]	**ANCIIRCoeffLSB[7:0]** Sets the LSB of the ANC FIR coefficients, it updates the 16 bits coefficient and it increases the coefficient pointer. The FIR coefficients are 44 and they are written sequentially from 0 to 43. The coefficient bank must be written setting first ‘ANCIIRUpDate’=1 and it is applied when the last coefficient is written. When ‘ANCIIRUpDate’ is set to zero the coefficient pointer is reset. A special procedure is used for the first IIR coefficients writing: ‘ANCIIRInit’ is set to “1” and then to “0”, then the 44 ANCIIRCoeff are written keeping ‘ANCIIRUpDate’=0.

ANCConf9 ANC Warp delay MSB

7	6	5	4	3	2	1	0
ANCWarpDelMSB[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D5B

Type: R/W

Reset: 0x00

Description: ANC Warp delay filter coefficient MSB part

[7:0]	**ANCWarpDelMSB[7:0]** Sets the MSB of the ANC warped delay line, the 16 bits coefficient is updated when the LSB part is written. (see ANCConf10 register for details)

ANCConf10 ANC Warp delay LSB

7	6	5	4	3	2	1	0
ANCWarpDelLSB[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D5C

Type: R/W

Reset: 0x00

Description: ANC Warp delay filter coefficient LSB part

[7:0]	**ANCWARPDelLSB[7:0]** Sets the LSB of the ANC warped delay line coefficients, it updates the 16-bits coefficient.

ANCConf11 ANC FIR peak register MSB

7	6	5	4	3	2	1	0
ANCFIRPeakMSB[7:0]							
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0D5D

Type: R

Reset: 0x00

Description: Monitor of ANC FIR output., MSB part.

[7:0]	**ANCFIRPeakMSB[7:0]** MSB of ANC FIR peak output. Note: The ANCConf12 and ANCConf11 register contents are cleared on ANCConf12 register reading so ANCConf11 register must be read first.

ANCConf12 ANC FIR peak register LSB

7	6	5	4	3	2	1	0
ANCFIRPeakLSB[7:0]							
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0D5E

Type: R

Reset: 0x00

Description: Monitor of ANC FIR output., LSB part.

[7:0]	**ANCFIRPeakLSB[7:0]** LSB of ANC FIR peak output. Note: The ANCConf12 and ANCConf11 register contents are cleared on ANCConf12 register reading.

ANCConf13 ANC IIR peak register. MSB part

7	6	5	4	3	2	1	0
ANCIIRPeakMSB[7:0]							
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0D5F

Type: R

Reset: 0x00

Description: Monitor of ANC IIR output.

[7:0]	**ANCIIRPeakMSB[7:0]** MSB of ANC IIR peak output. Note: The ANCConf14 and ANCConf13 register contents are cleared on ANCConf14 register reading so ANCConf13 register must be read first.

ANCConf14 ANC IIR peak register. LSB part

7	6	5	4	3	2	1	0
ANCIIRPeakLSB[7:0]							
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0D60

Type: R

Reset: 0x00

Description: Monitor of ANC IIR output.

[7:0]	**ANCIIRPeakLSB[7:0]** LSB of ANC IIR peak output Note: The ANCConf14 and ANCConf13 register contents are cleared on ANCConf14 register reading.

Side-tone FIR Control

SidFIRAdr — Side tone FIR address

7	6	5	4	3	2	1	0
FIRSidSet	FIRSidAddr[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D61

Type: R/W

Reset: 0x00

Description: Side Tone FIR memory address for filter coefficients

[7]	**FIRSidSet** 0: Last FIR coefficients not applied. 1: Applies the last programmed set of FIR coefficients.
[6:0]	**FIRSidAddr[6:0]** Set the 7 bits address of FIR coefficient that will be written

SidFIRCoef1 — Side tone FIR coefficient MSB

7	6	5	4	3	2	1	0
FIRSidCoeffMSB[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D62

Type: R/W

Reset: 0x00

Description: ST FIR memory for filter coefficient, MSB part

[7:0]	**FIRSidCoeffMSB[7:0]** Sets the MSB of the ST FIR coefficient at FIRSidAddr address. The whole coefficient is applied when LSB part is written. See FIRSidCoeffLSB[7:0] for details.

SidFIRCoef2 — Side tone FIR coefficient LSB

7	6	5	4	3	2	1	0
FIRSidCoeffLSB[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D63

Type: R/W

Reset: 0x00

Description: ST FIR memory for filter coefficient, LSB part

[7:0]	**FIRSidCoeffLSB[7:0]** Sets the LSB of the ST FIR coefficients at FIRSidAddr address, it updates the 16-bit coefficient and increments FIRSidAddr by 1 for burst programming. Reading does not affect the FIRSidAddr address pointer. Written coefficients are applied to filter just when' FIRSidSet' bit is set.

SidFIRConf — Filters control

7	6	5	4	3	2	1	0
Reserved					EnFIRSidS	FIRSidSToIF1	FIRSidBusy
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D64

Type: R/W

Reset: 0x00

Description: ANC and FIR filters status and control registers

[7:3]	Reserved
[2]	**EnFIRSidS** 0: ST FIR Filters are disabled. 1: ST FIR Filters are enabled.
[1]	**FIRSidSToIF1** 0: FIR1 and FIR2 Programmable filters run at AUD_IF0 frame sync. 1: FIR1 and FIR2 Programmable filters run at AUD_IF1 frame sync.
[0]	**FIRSidBusy** 0: The ST FIR is ready for new coefficients. 1: The new ST FIR coefficients are not applied yet.

Audio interrupts

AudIntMask1 — Interrupt mask

7	6	5	4	3	2	1	0
HsOffStMask	FifoFullMask	FifoEmptyMask	DASatMask	ADSatMask	ADDspMask	DADspMask	FIRSidMask
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D65

Type: R/W

Reset: 0x00

Description: interrupt request mask; LSB register

[7]	**HsOffStMask** 0: Bit IT_HsOffSt cannot generate an Interrupt Request 1: Bit IT_HsOffSt can generate an Interrupt Request
[6]	**FifoFullMask** 0: Bit IT_FifoFull cannot generate an Interrupt Request 1: Bit IT_FifoFull can generate an Interrupt Request
[5]	**FifoEmptyMask** 0: Bit IT_FifoEmpty cannot generate an Interrupt Request 1: Bit IT_FifoEmpty can generate an Interrupt Request
[4]	**DASatMask** 0: Bit IT_DASat cannot generate an Interrupt Request 1: Bit IT_DASat can generate an Interrupt Request
[3]	**ADSatMask** 0: Bit IT_ADSat cannot generate an Interrupt Request 1: Bit IT_ADSat can generate an Interrupt Request
[2]	**ADDspMask** 0: Bit IT_ADDsp cannot generate an Interrupt Request 1: Bit IT_ADDsp can generate an Interrupt Request
[1]	**DADspMask** 0: Bit IT_DADsp cannot generate an Interrupt Request 1: Bit IT_DADsp can generate an Interrupt Request
[0]	**FIRSidMask** 0: Bit IT_FIRSid cannot generate an Interrupt Request 1: Bit IT_FIRSid can generate an Interrupt Request

AudIntSource1 Interrupt source

7	6	5	4	3	2	1	0
IT_HsOffSt	IT_FifoFull	IT_FifoEmpty	IT_DASat	IT_ADSat	IT_ADDsp	IT_DADsp	IT_FIRSid
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0D66

Type: R

Reset: 0x80

Description: interrupt request status low register, the register content is cleared on read

[7]	**IT_HsOffSt** 0: At least one of HS driver is ON 1: Both HS drivers are Off
[6]	**IT_FifoFull** 0: Burst FIFO is not full. 1: Burst FIFO full event has occurred.
[5]	**IT_FifoEmpty** 0: Burst FIFO is not empty. 1: Burst FIFO empty event has occurred.
[4]	**IT_DASat** 0: No saturation occurred 1:A saturation has occurred in DA gain
[3]	**IT_ADSat** 0: No saturation occurred 1: A saturation has occurred in AD gain
[2]	**IT_ADDsp** 0: No saturation occurred 1:A saturation has occurred in AD DSP
[1]	**IT_DADsp** 0: No saturation occurred 1: A saturation has occurred in DA DSP
[0]	**IT_FIRSid** 0: No saturation occurred 1: A saturation has occurred in the FIRS or in sidetone mixers

AudIntMask2 — Interrupt mask

7	6	5	4	3	2	1	0
VssReadyMask	Reserved				ShortHsLMask	ShortHfRMask	ShortEarMask
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D67

Type: R/W

Reset: 0x00

Description: interrupt request mask; MSB register

[7]	**VSSReadyMask** 0: Bit IT_VSSReady cannot generate an Interrupt Request 1: Bit IT_VSSReady can generate an Interrupt Request
[6:3]	Reserved
[2]	**ShortHsLMask** 0: Bit IT_ShortHsL cannot generate an Interrupt Request 1: Bit IT_ShortHsL can generate an Interrupt Request
[1]	**ShortHsRMask** 0: Bit IT_ShortHsR cannot generate an Interrupt Request 1: Bit IT_ShortHsR can generate an Interrupt Request
[0]	**ShortEarMask** 0: Bit IT_ShortEar cannot generate an Interrupt Request 1: Bit IT_ShortEar can generate an Interrupt Request

AudIntSource2 — Interrupt source

7	6	5	4	3	2	1	0
IT_VssReady	Reserved				IT_ShortHsL	IT_ShortHfR	IT_ShortEar
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0D68

Type: R

Reset: 0x00

Description: interrupt request status MSB register, the register content is cleared on read

[7]	**IT_VssReady** 0: VSS from charge pump is not ready. 1: VSS from charge pump is ready.
[6:3]	Reserved
[2]	**IT_ShortHsL** 0: No short circuit detected 1: Short circuit detected on HsL Output driver
[1]	**IT_ShortHsR** 0: No short circuit detected 1: Short circuit detected on HsR Output driver
[0]	**IT_ShortEar** 0: No short circuit detected 1: Short circuit detected on Ear Output driver

Burst FIFO Control

FIFOConf1 — Burst FIFO control

7	6	5	4	3	2	1	0
BFIFOMask	BFIFO19M2	BFIFOInt[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D69

Type: R/W

Reset: 0x00

Description: Burst FIFO control register.

[7]	**BFIFOMask** 0: AD_DATA0 is unmasked in burst mode, it can wake up the digital audio data source 1: AD_DATA0 is masked in burst mode, it cannot wake up the digital audio data source
[6]	**BFIFO19M2** 0: BitClk0 frequency in burst mode is 38.4 MHz 1: BitClk0 frequency in burst mode is 19.2 MHz
[5:0]	**BFIFOInt[5:0]** 000000: No wakeup signal is generated 000001: Wakeup signal is generated when burst FIFO has less than 8 samples 000010: Wakeup signal is generated when burst FIFO has less than 16 samples .....: 111111: Wakeup signal is generated when burst FIFO has less than 504 samples

FIFOConf2 — Burst FIFO length

7	6	5	4	3	2	1	0
BFIFOTx[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D6A

Type: R/W

Reset: 0x00

Description: Burst FIFO length register. It define the burst transfer length in master mode.

[7:0]	**BFIFOTx[7:0]** This bit is valid in master mode. 00000000: No data requested from FIFO wakeup(1). 00000001: 8 samples burst requested from FIFO wakeup. 00000010: 16 samples burst requested from FIFO wakeup. .....: 11000000: 1536 samples(2) burst requested from FIFO wakeup. Full FIFO size. .....: 11111111: 2044 samples burst requested from FIFO wakeup.

1. Wake up: rising edge on AD_Data0 ball
2. It is possible to program FIFO depth values that exceed the FIFO size. This, however possible, can lead to FIFO-full condition and to audible artifacts. Note that the FIFO-full condition is possible also with BFIFOTx[7:0]<=1536 samples depending on the threshold of the FIFO interrupt request.

FIFOConf3 — Burst FIFO control

7	6	5	4	3	2	1	0
BFIFOExSl[2:0]			PreBitClk0[2:0]			BFIFOMast	BFIFORun
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D6B

Type: R/W

Reset: 0x00

Description: Burst FIFO control register.

[7:5]	**BFIFOExSl[2:0]** Number of extra slots in burst mode at the end of each frame 000: no extra slot 001: 1 extra slot 010: 2 extra slots .... 101: 5 extra slots 11x: 6 extra slots
[4:2]	**PreBitClk0[2:0]** Number of extra bit clocks that precede and follow the first Frame Sync on Aud_IF0 startup or Burst startup **Extra Bit Clocks** **Code / Before FSYNC0 / After last bit sent** 0000 0 0011 3 0102 4 0113 5 1004 6 1015 7 1106 8 1117 9
[1]	**BFIFOMast** 0: Burst FIFO interface is configured in slave mode 1: Burst FIFO interface is configured in master mode
[0]	**BFIFORun** 0: Burst FIFO interface is disabled 1: Burst FIFO interface is enabled This bit is an asynchronous enable/disable of the burst FIFO block clock. Use the 'IF0BFifoEn' bit (*DigIFConf3* register) to enable/disable the burst mode.

FIFOConf4 — Burst FIFO switch frame

7	6	5	4	3	2	1	0
BFIFOFramSw[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D6C

Type: R/W

Reset: 0x00

Description: Burst FIFO switch frame number.

[7:0]	**BFIFOFramSw[7:0]** It indicates on which frame number the switch from normal to burst mode will happen. The frame number is BFIFOFramSw*8. The switch occurs when the register content multiplied by 8 matches for the first time an 11 bits internal frame counter (FN, with wrap-around at 2047-0) that is reset each time the interface starts or is switched to normal mode. The frame where FN = BFIFOFramSw*8 will be the last one in normal mode, the frame where FN = BFIFOFramSw*8 + 1 will be the first one in burst mode.

FIFOConf5 — Burst FIFO wake up delay

7	6	5	4	3	2	1	0
BFIFOWakeUp[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D6D

Type: R/W

Reset: 0x00

Description: Burst FIFO wake up register.

[7:0]	**BFIFOWakUp** It indicates the delay from wake up generation to the start of burst transmission.(1) This delay does not happen on the first burst transmission. The delay is 26.7 µs*BFIFOWakUp.

1. Wake up: rising edge on AD_Data0 ball

FIFOConf6 — Burst FIFO samples number

7	6	5	4	3	2	1	0
BFIFOSample[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0D6E

Type: R

Reset: 0x00

Description: Number of samples currently in burst FIFO.

[7:0]	**BFIFOSample[7:0]** Number of samples currently present in burst FIFO is BFIFOSample*8.

Audio module revision

AudRev — Audio module revision

7	6	5	4	3	2	1	0
Reserved			AudIPRev[4:0]				
R	R	R	R	R	R	R/W	R/W

Address: BaseAddress: 0x0D6F

Type: R

Reset: 0x03 (cut 2.0)

Description: Audio module revision

[7:5]	Reserved
[4:0]	**AudIPRev[4:0]** Audio module revision 00000: AB8500 Early drop 00001: AB8500 cut 1.0 00010: AB8500 cut 2.0

4.4.11 Interrupt: Bank 0x0E

ITSource1 **ITSource1**

7	6	5	4	3	2	1	0
PonKey1db	Reserved	PonKey2db	Reserved	TempWarn	PlugTVDet	Reserved	MainExtCh NotOK
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E00

Type: R

Reset: 0xF0 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	**PonKey1db** 0: Inactive 1: PonKey1 ball level change detected
[6]	Reserved
[5]	**PonKey2db** 0: Inactive 1: PonKey2 ball level change detected
[4]	Reserved
[3]	**TempWarn** 0: Inactive 1: Die temperature higher than thermal warning threshold detected
[2]	**PlugTVdet** 0: Inactive 1: Tvset (75 Ω) connection/disconnection on CVBS ball detected
[1]	Reserved
[0]	**MainExtChNotOK** 0: Inactive 1: Main charger connected is not an allowed one (Main charger voltage above MainChOVVLow (10 V) or AC rectifier type charger detected) Charger is disabled

ITSource2 ITSource2

7	6	5	4	3	2	1	0
VbusDet	Reserved			MainCh PlugDet	Reserved		BattOVV
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E01

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	**VbusDet** 0: Inactive 1: Vbus ball level change detected
[6:4]	Reserved
[3]	**MainChPlugDet** 0: Inactive 1: Main charger plug/unplug detected
[2:1]	Reserved
[0]	**BattOVV** 0: Inactive 1: VbatA ball goes upper over voltage threshold (charge stopped)

ITSource3 ITSource3

7	6	5	4	3	2	1	0
MainChDropEnd	VbusOVV	ChWDExp	BatCtrlndb	Reserved	RtcAlarm	Rtc60s	VbusChDropEnd
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E02

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	**MainChDropEnd** 0: Main charger is not in dropout 1: Main charger was in dropout and internal input current loop update current regulation to avoid main charger to drop
[6]	**VbusOVV** 0: Inactive 1: Overvoltage on Vbus ball detected (USB charge is stopped)
[5]	**ChWDexp** 0: Inactive 1: Watchdog charger expiration detected (charge is stopped)
[4]	**BatCtrlndb** (not debounced signal) 0: Battery is present 1: Battery is removed (SIM interface powered down and charge stopped)
[3]	Reserved
[2]	**RtcAlarm** 0: Inactive 1: RTC timer reaches alarm time
[1]	**Rtc60s** 0: Inactive 1: RTC timer reaches a 60s period
[0]	**VbusChDropEnd** 0: USB charger is not in dropout 1: USB charger was in dropout and internal input current loop update current regulation to avoid USB charger to drop

ITSource4 ITSource4

7	6	5	4	3	2	1	0
BupChg	Reserved	LowBat	Reserved	CCIntCalib	CCEOC	IntAud	CCNConvAccu
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E03

Type: R

Reset: 0x32 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	**BupChg** 0: Inactive 1: BackUpBat ball voltage reaches *RtcBackupChg* register programmed voltage value
[6]	Reserved
[5]	**LowBat** 0:VbatA ball voltage below LowBat register programmed threshold 1: VbatA ball voltage above LowBat register programmed threshold
[4]	Reserved
[3]	**CCIntCalib** 0: Inactive 1: Coulomb Counter has ended its calibration
[2]	**CCEOC** 0: Inactive 1: Coulomb Counter has ended data conversion
[1]	**IntAud** 0: Audio interrupt from audio digital part detected 1: Inactive
[0]	**CCNConvAccu** 0: Inactive 1: Accumulation of N sample conversion is reached

ITSource5 ITSource5

7	6	5	4	3	2	1	0
GPADCSwConvEnd	AccDetect21db	Reserved	AccDetect22db	Reserved	AccDetect1db	Reserved	GPADCHwConvEnd
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E04

Type: R

Reset: 0xE1 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	**GPADCSwConfEnd** 0: Inactive 1: GP ADC conversion requested through software control is ended (data are available)
[6]	**AccDetect21db** 0: Inactive 1: AccDetect2 ball voltage level reaches *AccDetect21Th[3:0]* programmed threshold in *AccDetect2Th* register
[5]	Reserved
[4]	**AccDetect22db** 0: Inactive 1: AccDetect2 ball voltage level reaches *AccDetect22Th[3:0]* programmed threshold in *AccDetect2Th* register
[3]	Reserved
[2]	**AccDetect1db** 0: Inactive 1: AccDetect1 ball voltage level reaches *AccDetect1Th[3:0]* programmed threshold in *AccDetectDb1Th* register
[1]	Reserved
[0]	**GPADCHwConfEnd** 0: Inactive 1: GP ADC conversion requested through Hardware control (GPADCTrig ball) is ended (data are available)

ITSource7 ITSource7

7	6	5	4	3	2	1	0
Gpio13	Gpio12	Gpio11	Gpio10	Gpio9	Gpio8	Gpio7	Gpio6
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E06

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	**Gpio13** 0: Inactive 1: Edge detected on GPIO13 ball
[6]	**Gpio12** 0: Inactive 1: Edge detected on GPIO12 ball
[5]	**Gpio11** 0: Inactive 1: Edge detected on GPIO11 ball
[4]	**Gpio10** 0: Inactive 1: Edge detected on GPIO10 ball
[3]	**Gpio9** 0: Inactive 1: Edge detected on GPIO9 ball
[2]	**Gpio8** 0: Inactive 1: Edge detected on GPIO8 ball
[1]	**Gpio7** 0: Inactive 1: Edge detected on GPIO7 ball
[0]	**Gpio6** 0: Inactive 1: Edge detected on GPIO6 ball

ITSource8 ITSource8

7	6	5	4	3	2	1	0
Gpio41	Gpio40	Gpio39	Gpio38	Gpio37	Gpio36	Gpio25	Gpio24
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E07

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	**Gpio41** 0: Inactive 1: Edge detected on GPIO41 ball
[6]	**Gpio40** 0: Inactive 1: Edge detected on GPIO40 ball
[5]	**Gpio39** 0: Inactive 1: Edge detected on GPIO39 ball
[4]	**Gpio38** 0: Inactive 1: Edge detected on GPIO38 ball
[3]	**Gpio37** 0: Inactive 1: Edge detected on GPIO37 ball
[2]	**Gpio36** 0: Inactive 1: Edge detected on GPIO36 ball
[1]	**Gpio25** 0: Inactive 1: Edge detected on GPIO25 ball
[0]	**Gpio24** 0: Inactive 1: Edge detected on GPIO24 ball

ITSource10 ITSource12

7	6	5	4	3	2	1	0
UsbLinkStatus	Reserved		AdpSenseOff	AdpProbe UnPlug	AdpProbePlug	AdpSinkError	AdpSourceError
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E09

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	**UsbLinkStatus** 0: USBlink status value unchanged 1: USBlink status value changed
[6:5]	Reserved
[4]	**AdpSenseOff** 0: ADP sensing running 1: ADP sensing failed (no ADP probing detection detected within 3 s)
[3]	**AdpProbeUnPlug** 0: Previous state 1: Accessory unplug on Vbus
[2]	**AdpProbePlug** 0: Previous state 1: Accessory plug on Vbus
[1]	**AdpSinkError** 0: Inactive 1: No detection after 2046 x 32 kHz periods (about 62 ms)
[0]	**AdpSourceError** 0: Inactive 1: No detection after 2046 x 32 kHz periods (about 62 ms)

ITSource19 ITSource19

7	6	5	4	3	2	1	0
Reserved				BtempHigh	BtempMedium High	BtempLow Medium	BtempLow
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E12

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7:4]	Reserved
[3]	**BtempHigh** 0: Btemp < BtempHigh 1: Btemp > BtempHigh
[2]	**BtempMediumHigh** 0: Btemp < BtempMedium or Btemp > BtempHigh 1: BtempHigh > Btemp > BtempMedium
[1]	**BtempLowMedium** 0: Btemp < BtempLow or Btemp > BtempMedium 1: BtempMedium > Btemp > BtempLow
[0]	**BtempLow** 0: Btemp > BtempLow 1: BtempLow > Btemp

ITSource20 ITSource20

7	6	5	4	3	2	1	0
IDDetR4	IDDetR3	IDDetR2	IDDetR1	Reserved	IDWakeUp	UsbCharger NotOK	SRPDetect
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E13

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	**IDDetR4** 0: Inactive 1: R4(220 kΩ) ID resistance comparator threshold reached
[6]	**IDDetR3** 0: Inactive 1: R3(125 kΩ) ID resistance comparator threshold reached
[5]	**IDDetR2** 0: Inactive 1: R2(69 kΩ) ID resistance comparator threshold reached
[4]	**IDDetR1** 0: Inactive 1: R1(37 kΩ) ID resistance comparator threshold reached
[3]	Reserved
[2]	**IDWakeUp** 0: Inactive 1: Edge detected on ID
[1]	**UsbChargerNotOK** 0: Inactive 1: Not allowed USB charger detected
[0]	**SRPDetect** 0: Inactive 1: SRP detected

ITSource21 ITSource21

7	6	5	4	3	2	1	0
ChStopBySec	Reserved						
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E14

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	**ChStopBySec** 0: Charging is not stopped by a security reason 1: Charging is stopped by a security reason: - Battery temperature out of charging range - USB Charging mode: Combo Thermal Shutdown or VBUS OVV or VBUS below detection level (even if it is for less than 300 ms) - Main Charging mode: Main Charger Thermal Shutdown or Main OVV or Main below detection level (even if it is for less than 300 ms)

ITSource22 ITSource22

7	6	5	4	3	2	1	0
Reserved	ChCurLim HsChirp	Reserved		MainChThProt	Reserved	UsbChThProt	Reserved
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E15

Type: R

Reset: 0x80 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7]	Reserved
[6]	**ChCurLimHsChirp** 0: Inactive 1: Charging current is limited in HS or Chirp mode
[5:4]	Reserved
[3]	**MainChThProt** 0: Die temperature is not above the main charger thermal protection threshold (charge stopped) 1: Die temperature is above the main charger thermal protection threshold (charge stopped)
[2]	Reserved
[1]	**UsbChThProt** 0: Die temperature is not above the USB charger thermal protection threshold (charge stopped) 1: Die temperature is above the USB charger thermal protection threshold (charge stopped)
[0]	Reserved

ITLatch1 ITLatch1

7	6	5	4	3	2	1	0
IT_PonKey1dbR	IT_PonKey1dbF	IT_PonKey2dbR	IT_PonKey2dbF	IT_TempWarn	IT_PlugTVDet	IT_UnPlugTVDet	IT_Main ExtChNotOK
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E20

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_PonKey1dbR** 0: Inactive 1: Rising edge on PonKey1 ball detected
[6]	**IT_PonKey1dbF** 0: Inactive 1: Falling edge on PonKey1 ball detected
[5]	**IT_PonKey2dbR** 0: Inactive 1: Rising edge on PonKey2 ball detected
[4]	**IT_PonKey2dbF** 0: Inactive 1: Falling edge on PonKey2 ball detected
[3]	**IT_TempWarn** 0: Inactive 1: Die temperature higher than thermal warning threshold detected
[2]	**IT_PlugTVdet** 0: Inactive 1: Tvset (75 Ohms) connection on CVBS ball detected
[1]	**IT_UnPlugTVdet** 0: Inactive 1: Tvset (75 Ohms) disconnection on CVBS ball detected
[0]	**IT_MainExtChNotOK** 0: Inactive 1: Not allowed main charger detected on MainCh ball (Main charger voltage above MainChOVVLow (10 V) or AC rectifier type charger detected) Charger is disabled

ITLatch2 ITLatch2

7	6	5	4	3	2	1	0
IT_VbusDetR	IT_VbusDetF	Reserved		IT_MainCh PlugDet]	IT_MainCh UnPlugDet]	Reserved	IT_BattOVV
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E21

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_VbusDetR** 0: Inactive 1: Rising edge on Vbus ball detected
[6]	**IT_VbusDetF** 0: Inactive 1: Falling edge on Vbus ball detected
[5:4]	Reserved
[3]	**IT_MainChPlugDet** 0: Inactive 1: Main charger plug detected
[2]	**IT_MainChUnPlugDet** 0: Inactive 1: Main charger unplug detected
[1]	Reserved
[0]	**IT_BattOVV** 0: Inactive 1: VbatA ball goes above voltage threshold (charge stopped)

ITLatch3 ITLatch3

7	6	5	4	3	2	1	0
IT_MainCh DropEnd	IT_VbusOVV	IT_ChWDExp	IT_BatCtrlndb	Reserved	IT_RtcAlarm	IT_Rtc60s	IT_VbusCh DropEnd
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E22

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_MainChDropEnd** 0: Inactive 1: Main charger was in dropout and internal input current loop update current regulation to avoid main charger to drop
[6]	**IT_VbusOVV** 0: Inactive 1: Overvoltage on Vbus ball detected (USB charge is stopped)
[5]	**IT_ChWDexp** 0: Inactive 1: Watchdog charger expiration detected (charge is stopped)
[4]	**IT_BatCtrlndb** 0: Inactive 1: Battery removal detected (SIM interface powered down & charge stopped)
[3]	Reserved
[2]	**IT_RtcAlarm** 0: Inactive 1: RTC timer reaches alarm time
[1]	**IT_Rtc60s** 0: Inactive 1: RTC timer reaches a 60 s period
[0]	**IT_VbusChDropEnd** 0: Inactive 1: USB charger was in dropout and internal input current loop update current regulation to avoid USB charger to drop

ITLatch4 ITLatch4

7	6	5	4	3	2	1	0
IT_BupChgOk	IT_BupChgNok	IT_LowBatR	IT_LowBatF	IT_CCIntCalib	IT_CCEOC	IT_IntAud	IT_CCNConv Accu
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E23

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_BupChgOk** 0: Inactive 1: BackUpBat ball voltage goes above *RtcBackupChg* register programmed voltage value
[6]	**IT_BupChgNok** 0: Inactive 1: BackUpBat ball voltage goes below *RtcBackupChg* register programmed voltage value
[5]	**IT_LowBatR** 0: Inactive 1: VbatA ball voltage goes above LowBat register programmed threshold
[4]	**IT_LowBatF** 0: Inactive 1: VbatA ball voltage goes below LowBat register programmed threshold
[3]	**IT_CCIntCalib** 0: Inactive 1: Coulomb Counter has ended its calibration
[2]	**IT_CCEOC** 0: Inactive 1: Coulomb Counter has ended data conversion
[1]	**IT_IntAud** 0: Inactive 1: Audio interrupt form audio digital part detected
[0]	**IT_CCNconvAccu** 0: Inactive 1: Accumulation of N sample conversion is detected

ITLatch5 ITLatch5

7	6	5	4	3	2	1	0
IT_GPADCSw ConvEnd	IT_Acc Detect21dbR	IT_Acc Detect21dbF	IT_Acc Detect22dbR	IT_Acc Detect22dbF	IT_Acc Detect1dbR	IT_Acc Detect1dbF	IT_GPADCHw ConvEnd
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E24

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_GPADCSwConfEnd** 0: Inactive 1: GP ADC conversion requested through software control is ended (data are available)
[6]	**IT_AccDetect21dbF** 0: Inactive 1: AccDetect2 ball voltage level goes below *AccDetect21Th[3:0]* register programmed threshold in *AccDetect2Th* register
[5]	**IT_AccDetect21dbR** 0: Inactive 1: AccDetect2 ball voltage level goes above *AccDetect21Th[3:0]* register programmed threshold in *AccDetect2Th* register
[4]	**IT_AccDetect22dbF** 0: Inactive 1: AccDetect2 ball voltage level goes below *AccDetect22Th[3:0]* register programmed threshold in *AccDetect2Th* register
[3]	**IT_AccDetect22dbR** 0: Inactive 1: AccDetect2 ball voltage level goes above *AccDetect22Th[3:0]* register programmed threshold in *AccDetect2Th* register
[2]	**IT_AccDetect1dbR** 0: Inactive 1: AccDetect1 ball voltage level goes above *AccDetect1Th[3:0]* register programmed threshold in *AccDetectDb1Th* register
[1]	**IT_AccDetect1dbF** 0: Inactive 1: AccDetect1 ball voltage level goes below *AccDetect1Th[3:0]* register programmed threshold in *AccDetectDb1Th* register
[0]	**IT_GPADCHwConvEnd** 0: Inactive 1: GP ADC conversion requested through Hardware control (GPADCTrig ball) is ended (data are available)

ITLatch7 ITLatch7

7	6	5	4	3	2	1	0
IT_Gpio13R	IT_Gpio12R	IT_Gpio11R	IT_Gpio10R	IT_Gpio9R	IT_Gpio8R	IT_Gpio7R	IT_Gpio6R
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E26

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_Gpio13R** 0: Inactive 1: Rising edge detected on GPIO13 ball
[6]	**IT_Gpio12R** 0: Inactive 1: Rising edge detected on GPIO12 ball
[5]	**IT_Gpio11R** 0: Inactive 1: Rising edge detected on GPIO11 ball
[4]	**IT_Gpio10R** 0: Inactive 1: Rising edge detected on GPIO10 ball
[3]	**IT_Gpio9R** 0: Inactive 1: Rising edge detected on GPIO9 ball
[2]	**IT_Gpio8R** 0: Inactive 1: Rising edge detected on GPIO8 ball
[1]	**IT_Gpio7R** 0: Inactive 1: Rising edge detected on GPIO7 ball
[0]	**IT_Gpio6R** 0: Inactive 1: Rising edge detected on GPIO6 ball

ITLatch8 ITLatch8

7	6	5	4	3	2	1	0
IT_Gpio41R	IT_Gpio40R	IT_Gpio39R	IT_Gpio38R	IT_Gpio37R	IT_Gpio36R	IT_Gpio25R	IT_Gpio24R
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E27

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_Gpio41R** 0: Inactive 1: Rising edge detected on GPIO41 ball
[6]	**IT_Gpio40R** 0: Inactive 1: Rising edge detected on GPIO40 ball
[5]	**IT_Gpio39R** 0: Inactive 1: Rising edge detected on GPIO39 ball
[4]	**IT_Gpio38R** 0: Inactive 1: Rising edge detected on GPIO38 ball
[3]	**IT_Gpio37R** 0: Inactive 1: Rising edge detected on GPIO37 ball
[2]	**IT_Gpio36R** 0: Inactive 1: Rising edge detected on GPIO36 ball
[1]	**IT_Gpio25R** 0: Inactive 1: Rising edge detected on GPIO25 ball
[0]	**IT_Gpio24R** 0: Inactive 1: Rising edge detected on GPIO24 ball

ITLatch9 ITLatch9

7	6	5	4	3	2	1	0
IT_Gpio13F	IT_Gpio12F	IT_Gpio11F	IT_Gpio10F	IT_Gpio9F	IT_Gpio8F	IT_Gpio7F	IT_Gpio6F
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E28

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_Gpio13F** 0: Inactive 1: Falling edge detected on GPIO13 ball
[6]	**IT_Gpio12F** 0: Inactive 1: Falling edge detected on GPIO12 ball
[5]	**IT_Gpio11F** 0: Inactive 1: Falling edge detected on GPIO11 ball
[4]	**IT_Gpio10F** 0: Inactive 1: Falling edge detected on GPIO10 ball
[3]	**IT_Gpio9F** 0: Inactive 1: Falling edge detected on GPIO9 ball
[2]	**IT_Gpio8F** 0: Inactive 1: Falling edge detected on GPIO8 ball
[1]	**IT_Gpio7F** 0: Inactive 1: Falling edge detected on GPIO7 ball
[0]	**IT_Gpio6F** 0: Inactive 1: Falling edge detected on GPIO6 ball

ITLatch10 ITLatch10

7	6	5	4	3	2	1	0
IT_Gpio41F	IT_Gpio40F	IT_Gpio39F	IT_Gpio38F	IT_Gpio37F	IT_Gpio36F	IT_Gpio25F	IT_Gpio24F
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E29

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_Gpio41F** 0: Inactive 1: Falling edge detected on GPIO41 ball
[6]	**IT_Gpio40F** 0: Inactive 1: Falling edge detected on GPIO40 ball
[5]	**IT_Gpio39F** 0: Inactive 1: Falling edge detected on GPIO39 ball
[4]	**IT_Gpio38F** 0: Inactive 1: Falling edge detected on GPIO38 ball
[3]	**IT_Gpio37F** 0: Inactive 1: Falling edge detected on GPIO37 ball
[2]	**IT_Gpio36F** 0: Inactive 1: Falling edge detected on GPIO36 ball
[1]	**IT_Gpio25F** 0: Inactive 1: Falling edge detected on GPIO25 ball
[0]	**IT_Gpio24F** 0: Inactive 1: Falling edge detected on GPIO24 ball

ITLatch12 ITLatch12

7	6	5	4	3	2	1	0
IT_UsbLink Status	IT_UsbPhy PowerError	Reserved	IT_AdpSenseOff	IT_AdpProbe UnPlug	IT_AdpProbe Plug	IT_AdpSink Error	IT_AdpSource Error
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E2B

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_UsbLinkStatus** 0: Inactive 1: Usblink status value has changed
[6]	**IT_UsbPhyPowerError** 0: Inactive 1: USB PHY has been reset due to a power loss
[5]	Reserved
[4]	**IT_AdpSenseOff** 0: Inactive 1: ADP sensing failed (no ADP probing detected within 3 s)
[3]	**IT_AdpProbeUnPlug** 0: Inactive 1: Accessory unplug on Vbus
[2]	**IT_AdpProbePlug** 0: Inactive 1: Accessory plug on Vbus
[1]	**IT_AdpSinkError** 0: Inactive 1: No detection after 2046 x 32 kHz periods (about 62 ms)
[0]	**IT_AdpSourceError** 0: Inactive 1: No detection after 2046 x 32 kHz periods (about 62 ms)

ITLatch19 ITLatch19

7	6	5	4	3	2	1	0
Reserved				IT_BTemp High	IT_BTemp MediumHigh	IT_BTemp LowMedium	IT_BTemp Low
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E32

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Source interrupts

[7:4]	Reserved
[3]	**IT_BtempHigh** 0: Inactive 1: Btemp > BtempHigh detected
[2]	**IT_BtempMediumHigh** 0: Inactive 1: BtempHigh > Btemp > BtempMedium detected
[1]	**IT_BtempLowMedium** 0: Inactive 1: BtempMedium > Btemp > BtempLow detected
[0]	**IT_BtempLow** 0: Inactive 1: Btemp <BtempLow detected

ITLatch20 ITLatch20

7	6	5	4	3	2	1	0
IT_IDDetR4R	IT_IDDetR3R	IT_IDDetR2R	IT_IDDetR1R	Reserved	IT_IDWakeUpR	IT_Usb ChargerNotOKR	IT_SRPDetect
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E33

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_IDDetR4R** 0: Inactive 1: ID resistance greater than R4(220 kΩ) detected
[6]	**IT_IDDetR3R** 0: Inactive 1: ID resistance greater than R3(125 kΩ) detected
[5]	**IT_IDDetR2R** 0: Inactive 1: ID resistance greater than R2(69 kΩ) detected
[4]	**IT_IDDetR1R** 0: Inactive 1: ID resistance greater than R1(37 kΩ) detected
[3]	Reserved
[2]	**IT_IDWakeUpR** 0: Inactive 1: Rising edge detected on ID
[1]	**IT_UsbChargerNotOKR** 0: Inactive 1: Not allowed USB charger detected on Vbus ball
[0]	**IT_SRPDetect** 0: Inactive 1: SRP detected

ITLatch21 ITLatch21

7	6	5	4	3	2	1	0
IT_ChStopBySec	IT_ChAuto RestartAftSec	IT_IDDetR4F	IT_IDDetR3F	IT_IDDetR2F	IT_IDDetR1F	Reserved	IT_IDWakeUpF
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E34

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_ChStopBySec** 0: Inactive 1: Charging is stopped by security reason: - Battery temperature out of charging range - USB Charging mode: Combo Thermal Shutdown or VBUS OVV or VBUS below detection level (even if it is for less than 300 ms) - Main Charging mode: Main Charger Thermal Shutdown or Main OVV or Main below detection level (even if it is for less than 300 ms)
[6]	**IT_ChAutoRestartAftSec** 0: Inactive 1: Charging has restarted after security reason
[5]	**IT_IDDetR4F** 0: Inactive 1: ID resistance lower than R4(220 kΩ) detected
[4]	**IT_IDDetR3F** 0: Inactive 1: ID resistance lower than R3(125 kΩ) detected
[3]	**IT_IDDetR2F** 0: Inactive 1: ID resistance lower than R2(69 kΩ) detected
[2]	**IT_IDDetR1F** 0: Inactive 1: ID resistance lower than R1(37 kΩ) detected
[1]	Reserved
[0]	**IT_IDWakeUpF** 0: Inactive 1: Falling edge detected on ID

ITLatch22 ITLatch22

7	6	5	4	3	2	1	0
IT_Xtal32kKO	IT_ChCurLim HsChirp	IT_ChCurLim NoHsChirp	Reserved	IT_MainChTh ProtR	IT_MainChTh ProtF	IT_UsbChTh ProtR	IT_UsbChTh ProtF
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E35

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Latched interrupts (cleared once reading)

[7]	**IT_Xtal32kKO** 0: Inactive 1: 32 kHz crystal oscillator has failed at start up
[6]	**IT_ChCurLimHsChirp** 0: Inactive 1: Charging current is limited in HS or Chirp mode
[5]	**IT_ChCurLimNoHsChirp** 0: Inactive 1: Charging current is not any more limited in HS or Chirp mode
[3]	**IT_MainChThProtR** 0: Inactive 1: Die temperature is higher than main charger thermal protection threshold (charge stopped)
[2]	**IT_MainChThProtF** 0: Inactive 1: Die temperature is lower than main charger thermal protection threshold (charge not stopped)
[1]	**IT_UsbChThProtR** 0: Inactive 1: Die temperature is higher than USB charger thermal protection threshold (charge stopped)
[0]	**IT_UsbChThProtF** 0: Inactive 1: Die temperature is lower than USB charger thermal protection threshold (charge not stopped)

ITMask1 ITMask1

7	6	5	4	3	2	1	0
MaskIT_ PonKey1dbR	MaskIT_ PonKey1dbF	MaskIT_ PonKey2dbR	MaskIT_ PonKey2dbF	MaskIT_ TempWarn	MaskIT_ PlugTVDet	MaskIT_ UnPlugTVDet	MaskIT_Main ExtChNotOK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E40

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_PonKey1dbR** 0: Inactive 1: Rising edge on PonKey1 ball Interrupt masked
[6]	**MaskIT_PonKey1dbF** 0: Inactive 1: Falling edge on PonKey1 ball Interrupt masked
[5]	**MaskIT_PonKey2dbR** 0: Inactive 1: Rising edge on PonKey2 ball Interrupt masked
[4]	**MaskIT_PonKey2dbF** 0: Inactive 1: Falling edge on PonKey2 ball Interrupt masked
[3]	**MaskIT_TempWarn** 0: Inactive 1: Die temperature higher than thermal warning threshold Interrupt masked
[2]	**MaskIT_PlugTVdet** 0: Inactive 1: Tvset (75 Ω) connection on CVBS ball Interrupt masked
[1]	**MaskIT_UnPlugTVdet** 0: Inactive 1: Tvset (75 Ω) disconnection on CVBS ball Interrupt masked
[0]	**MaskIT_MainExtChNotOK** 0: Inactive 1: Not allowed main charger detected on MainCh ball interrupt masked

ITMask2 ITMask2

7	6	5	4	3	2	1	0
MaskIT_ VbusDetR	MaskIT_ VbusDetF	Reserved		MaskIT_MainCh PlugDet	MaskIT_MainCh UnPlugDet	Reserved	MaskIT_ BattOVV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E41

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_VbusDetR** 0: Inactive 1: Rising edge on Vbus ball Interrupt masked
[6]	**MaskIT_VbusDetF** 0: Inactive 1: Falling edge on Vbus ball Interrupt masked
[5:4]	Reserved
[3]	**MaskIT_MainChPlugDet** 0: Inactive 1: Main charger plug Interrupt masked
[2]	**MaskIT_MainChUnPlugDet** 0: Inactive 1: Main charger unplug Interrupt masked
[1]	Reserved
[0]	**MaskIT_BattOVV** 0: Inactive 1: VbatA ball going upper over voltage threshold interrupt masked

ITMask3 ITMask3

7	6	5	4	3	2	1	0
MaskIT_ MainChDropEnd	MaskIT_ VbusOVV	MaskIT_ ChWDExp	MaskIT_ BatCtrlndb	Reserved	MaskIT_ RtcAlarm	MaskIT_Rtc60s	MaskIT_ VbusChDropEnd
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E42

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_MainChDropEnd** 0: Inactive 1: IT_MainChDropEnd masked
[6]	**MaskIT_VbusOVV** 0: Inactive 1: Overvoltage on Vbus ball Interrupt masked
[5]	**MaskIT_ChWDexp** 0: Inactive 1: Watchdog charger expiration Interrupt masked
[4]	**MaskIT_BatCtrlndb** 0: Inactive 1: Battery removal Interrupt masked
[3]	Reserved
[2]	**MaskIT_RtcAlarm** 0: Inactive 1: RTC timer reaches alarm time interrupt masked
[1]	**MaskIT_Rtc60s** 0: Inactive 1: RTC timer reaches a 60 s period interrupt masked
[0]	**MaskIT_VbusChDropEnd** 0: Inactive 1: IT_VbusChDropEnd masked

ITMask4 ITMask4

7	6	5	4	3	2	1	0
MaskIT_ BupChgOk	MaskIT_ BupChgNok	MaskIT_ LowBatR	MaskIT_ LowBatF	MaskIT_ CCIntCalib	MaskIT_CCEOC	MaskIT_IntAud	Mask IT_CCN ConvAccu
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E43

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_BupChgOk** 0: Inactive 1: BackUpBat ball voltage goes above *RtcBackupChg* register programmed voltage value, interrupt masked
[6]	**MaskIT_BupChgNok** 0: Inactive 1: BackUpBat ball voltage goes below *RtcBackupChg* register programmed voltage value, interrupt masked
[5]	**MaskIT_LowBatR** 0: Inactive 1: VbatA ball voltage goes above LowBat register programmed threshold, interrupt masked
[4]	**MaskIT_LowBatF** 0: Inactive 1: VbatA ball voltage goes below LowBat register programmed threshold, interrupt masked
[3]	**MaskIT_CCIntCalib** 0: Inactive 1: Coulomb Counter has ended its calibration, interrupt masked
[2]	**MaskIT_CCEOC** 0: Inactive 1: Coulomb Counter has ended data conversion, interrupt masked
[1]	**MaskIT_IntAud** 0: Inactive 1: Audio interrupt form audio digital part Interrupt masked
[0]	**MaskIT_CCNconvAccu** 0: Inactive 1: Accumulation of N sample conversion interrupt is masked

ITMask5 ITMask5

7	6	5	4	3	2	1	0
MaskIT_GPADC SwConvEnd	MaskIT_Acc Detect21dbR	MaskIT_Acc Detect21dbF	MaskIT_Acc Detect22dbR	MaskIT_Acc Detect22dbF	MaskIT_Acc Detect1dbR	MaskIT_Acc Detect1dbF	MaskIT_GPADC HwConvEnd
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E44

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_GPADCSwConfEnd** 0: Inactive 1: GP ADC conversion requested through software control is ended (data is available) interrupt masked
[6]	**MaskIT_AccDetect21dbF** 0: Inactive 1: AccDetect2 ball voltage level goes below *AccDetect21Th[3:0]* register programmed threshold in *AccDetect2Th* register, interrupt masked
[5]	**MaskIT_AccDetect21dbR** 0: Inactive 1: AccDetect2 ball voltage level goes above *AccDetect21Th[3:0]* register programmed threshold in *AccDetect2Th* register, interrupt masked
[4]	**MaskIT_AccDetect22dbF** 0: Inactive 1: AccDetect2 ball voltage level goes below *AccDetect22Th[3:0]* register programmed threshold in *AccDetect2Th* register, interrupt masked
[3]	**MaskIT_AccDetect22dbR** 0: Inactive 1: AccDetect2 ball voltage level goes above *AccDetect22Th[3:0]* register programmed threshold in *AccDetect2Th* register, interrupt masked
[2]	**MaskIT_AccDetect1dbR** 0: Inactive 1: AccDetect1 ball voltage level goes above *AccDetect1Th[3:0]* register programmed threshold in *AccDetectDb1Th* register, interrupt masked
[1]	**MaskIT_AccDetect1dbF** 0: Inactive 1: AccDetect1 ball voltage level goes below *AccDetect1Th[3:0]* register programmed threshold in *AccDetectDb1Th* register, interrupt masked
[0]	**MaskIT_GPADCHwConfEnd** 0: Inactive 1: GP ADC conversion requested through Hardware control (GPADCTrig ball) is ended (data are available) interrupt masked

ITMask7 ITMask7

7	6	5	4	3	2	1	0
MaskIT_ Gpio13R	MaskIT_ Gpio12R	MaskIT_ Gpio11R	MaskIT_ Gpio10R	MaskIT_ Gpio9R	MaskIT_ Gpio8R	MaskIT_ Gpio7R	MaskIT_ Gpio6R
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E46

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_Gpio13R** 0: Inactive 1: Rising edge Interrupt masked on GPIO13 ball
[6]	**MaskIT_Gpio12R** 0: Inactive 1: Rising edge Interrupt masked on GPIO12 ball
[5]	**MaskIT_Gpio11R** 0: Inactive 1: Rising edge Interrupt masked on GPIO11 ball
[4]	**MaskIT_Gpio10R** 0: Inactive 1: Rising edge Interrupt masked on GPIO10 ball
[3]	**MaskIT_Gpio9R** 0: Inactive 1: Rising edge Interrupt masked on GPIO9 ball
[2]	**MaskIT_Gpio8R** 0: Inactive 1: Rising edge Interrupt masked on GPIO8 ball
[1]	**MaskIT_Gpio7R** 0: Inactive 1: Rising edge Interrupt masked on GPIO7 ball
[0]	**MaskIT_Gpio6R** 0: Inactive 1: Rising edge Interrupt masked on GPIO6 ball

ITMask8 ITMask8

7	6	5	4	3	2	1	0
MaskIT_ Gpio41R	MaskIT_ Gpio40R	MaskIT_ Gpio39R	MaskIT_ Gpio38R	MaskIT_ Gpio37R	MaskIT_ Gpio36R	MaskIT_ Gpio25R	MaskIT_ Gpio24R
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E47

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_Gpio41R** 0: Inactive 1: Rising edge Interrupt masked on GPIO41 ball
[6]	**MaskIT_Gpio40R** 0: Inactive 1: Rising edge Interrupt masked on GPIO40 ball
[5]	**MaskIT_Gpio39R** 0: Inactive 1: Rising edge Interrupt masked on GPIO39 ball
[4]	**MaskIT_Gpio38R** 0: Inactive 1: Rising edge Interrupt masked on GPIO38 ball
[3]	**MaskIT_Gpio37R** 0: Inactive 1: Rising edge Interrupt masked on GPIO37 ball
[2]	**MaskIT_Gpio36R** 0: Inactive 1: Rising edge Interrupt masked on GPIO36 ball
[1]	**MaskIT_Gpio25R** 0: Inactive 1: Rising edge Interrupt masked on GPIO25 ball
[0]	**MaskIT_Gpio24R** 0: Inactive 1: Rising edge Interrupt masked on GPIO24 ball

ITMask9 ITMask9

7	6	5	4	3	2	1	0
MaskIT_ Gpio13F	MaskIT_ Gpio12F	MaskIT_ Gpio11F	MaskIT_ Gpio10F	MaskIT_ Gpio9F	MaskIT_ Gpio8F	MaskIT_ Gpio7F	MaskIT_ Gpio6F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E48

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_Gpio13F** 0: Inactive 1: Falling edge Interrupt masked on GPIO13 ball
[6]	**MaskIT_Gpio12F** 0: Inactive 1: Falling edge Interrupt masked on GPIO12 ball
[5]	**MaskIT_Gpio11F** 0: Inactive 1: Falling edge Interrupt masked on GPIO11 ball
[4]	**MaskIT_Gpio10F** 0: Inactive 1: Falling edge Interrupt masked on GPIO10 ball
[3]	**MaskIT_Gpio9F** 0: Inactive 1: Falling edge Interrupt masked on GPIO9 ball
[2]	**MaskIT_Gpio8F** 0: Inactive 1: Falling edge Interrupt masked on GPIO8 ball
[1]	**MaskIT_Gpio7F** 0: Inactive 1: Falling edge Interrupt masked on GPIO7 ball
[0]	**MaskIT_Gpio6F** 0: Inactive 1: Falling edge Interrupt masked on GPIO6 ball

ITMask10 ITMask10

7	6	5	4	3	2	1	0
MaskIT_ Gpio41F	MaskIT_ Gpio40F	MaskIT_ Gpio39F	MaskIT_ Gpio38F	MaskIT_ Gpio37F	MaskIT_ Gpio36F	MaskIT_ Gpio25F	MaskIT_ Gpio24F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E49

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_Gpio41F** 0: Inactive 1: Falling edge Interrupt masked on GPIO41 ball
[6]	**MaskIT_Gpio40F** 0: Inactive 1: Falling edge Interrupt masked on GPIO40 ball
[5]	**MaskIT_Gpio39F** 0: Inactive 1: Falling edge Interrupt masked on GPIO39 ball
[4]	**MaskIT_Gpio38F** 0: Inactive 1: Falling edge Interrupt masked on GPIO38 ball
[3]	**MaskIT_Gpio37F** 0: Inactive 1: Falling edge Interrupt masked on GPIO37 ball
[2]	**MaskIT_Gpio36F** 0: Inactive 1: Falling edge Interrupt masked on GPIO36 ball
[1]	**MaskIT_Gpio25F** 0: Inactive 1: Falling edge Interrupt masked on GPIO25 ball
[0]	**MaskIT_Gpio24F** 0: Inactive 1: Falling edge Interrupt masked on GPIO24 ball

ITMask12 ITMask12

7	6	5	4	3	2	1	0
MaskIT_Usb LinkStatus	MaskIT_UsbPhy PowerError	Reserved	MaskIT_Adp SenseOff	MaskIT_Adp ProbeUnPlug	MaskIT_Adp ProbePlug	MaskIT_Adp SinkError	MaskIT_Adp SourceError
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E4B

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_UsbLinkStatus** 0: Inactive 1: Usblink status value changed interrupt masked
[6]	**MaskIT_UsbPhyPowerError** 0: Inactive 1: USB PHY reset due to a power loss interrupt masked
[5]	Reserved
[4]	**MaskIT_AdpSenseOff** 0: Inactive 1: ADP sensing failed (no ADP probing detected within 3 s) interrupt masked
[3]	**MaskIT_AdpProbeUnPlug** 0: Inactive 1: Accessory unplug on Vbus interrupt masked
[2]	**MaskIT_AdpProbePlug** 0: Inactive 1: Accessory plug on Vbus interrupt masked
[1]	**MaskIT_AdpSinkError** 0: Inactive 1: No detection after 2046 x 32 kHz periods (about 62 ms) interrupt masked
[0]	**MaskIT_AdpSourceError** 0: Inactive 1: No detection after 2046 x 32 kHz periods (about 62 ms) interrupt masked

ITMask19 ITMask19

7	6	5	4	3	2	1	0
Reserved				MaskIT_BTemp High	MaskIT_BTemp MediumHigh	MaskIT_BTemp LowMedium	MaskIT_BTemp Low
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0E52

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7:4]	Reserved
[3]	**MaskIT_BtempHigh** 0: Inactive 1: Interrupt “Btemp > BtempHigh” masked
[2]	**MaskIT_BtempMediumHigh** 0: Inactive 1: Interrupt “BtempHigh > Btemp > BtempMedium” masked
[1]	**MaskIT_BtempLowMedium** 0: Inactive 1: Interrupt “BtempMedium > Btemp > BtempLow” masked
[0]	**MaskIT_BtempLow** 0: Inactive 1: Interrupt “Btemp <BtempLow” masked

ITMask20 ITMask20

7	6	5	4	3	2	1	0
MaskIT_ IDDetR4R	MaskIT_ IDDetR3R	MaskIT_ IDDetR2R	MaskIT_ IDDetR1R	Reserved	MaskIT_ IDWakeUpR	MaskIT_ UsbCharger NotOKR	MaskIT_ SRPDetect
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E53

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_IDDetR4R** 0: Inactive 1: ID resistance greater than R4(220 kΩ) detection masked
[6]	**MaskIT_IDDetR3R** 0: Inactive 1: ID resistance greater than R3(125 kΩ) detection masked
[5]	**MaskIT_IDDetR2R** 0: Inactive 1: ID resistance greater than R2(69 kΩ) detection masked
[4]	**MaskIT_IDDetR1R** 0: Inactive 1: ID resistance greater than R1(37 kΩ) detection masked
[3]	Reserved
[2]	**MaskIT_IDWakeUpR** 0: Inactive 1: Rising edge on ID Interrupt masked
[1]	**MaskIT_UsbChargerNotOKR** 0: Inactive 1: Not allowed USB charger detection on Vbus interrupt masked
[0]	**MaskIT_SRPDetect** 0: Inactive 1: SRP detect Interrupt masked

ITMask21 ITMask21

7	6	5	4	3	2	1	0
MaskIT_ChStop BySec	MaskIT_ChAuto RestartAftSec	MaskIT_ IDDetR4F	MaskIT_ IDDetR3F	MaskIT_ IDDetR2F	MaskIT_ IDDetR1F	Reserved	MaskIT_ IDWakeUpF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E54

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_ChStopBySec** 0: Inactive 1: Charging is stopped by security reason interrupt masked
[6]	**MaskIT_ChAutoRestartAftSec** 0: Inactive 1: Charging has restarted after security reason interrupt masked
[5]	**MaskIT_IDDetR4F** 0: Inactive 1: ID resistance lower than R4(220 kΩ) detection masked
[4]	**MaskIT_IDDetR3F** 0: Inactive 1: ID resistance lower than R3(125 kΩ) detection masked
[3]	**MaskIT_IDDetR2F** 0: Inactive 1: ID resistance lower than R2(69 kΩ) detection masked
[2]	**MaskIT_IDDetR1F** 0: Inactive 1: ID resistance lower than R1(37 kΩ) detection masked
[1]	Reserved
[0]	**MaskIT_IDWakeUpF** 0: Inactive 1: Falling edge on ID Interrupt masked

ITMask22 ITMask22

7	6	5	4	3	2	1	0
MaskIT_ Xtal32kKO	MaskIT_ChCur LimHsChirp	MaskIT_ChCur LimNoHsChirp	Reserved	MaskIT_Main ChThProtR	MaskIT_Main ChThProtF	MaskIT_Usb ChThProtR	MaskIT_Usb ChThProtF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E55

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Mask interrupts

[7]	**MaskIT_Xtal32kKO** 0: Inactive 1: 32 kHz crystal oscillator has failed at start up interrupt masked
[6]	**MaskIT_ChCurLimHsChirp** 0: Inactive 1: Charging current is limited in HS or Chirp mode interrupt masked
[5]	**MaskIT_ChCurLimNoHsChirp** 0: Inactive 1: Charging current is no longer limited in HS or Chirp mode interrupt masked
[4]	Reserved
[3]	**MaskIT_MainChThProtR** 0: Inactive 1: Die temperature is above main charger thermal protection threshold (charge stopped) interrupt masked
[2]	**MaskIT_MainChThProtF** 0: Inactive 1: Die temperature is below main charger thermal protection threshold (charge not stopped) interrupt masked
[1]	**MaskIT_UsbChThProtR** 0: Inactive 1: Die temperature is above USB charger thermal protection threshold (charge stopped) interrupt masked
[0]	**MaskT_UsbChThProtF** 0: Inactive 1: Die temperature is below USB charger thermal protection threshold (charge not stopped) interrupt masked

ITLatchHier1 — Hierarchical interrupt

7	6	5	4	3	2	1	0
ITFromLatch8	ITFromLatch7	Reserved	ITFromLatch5	ITFromLatch4	ITFromLatch3	ITFromLatch2	ITFromLatch1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E60

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Hierarchical interrupts

[7]	**ITFromLatch8** 0: Inactive 1: At least one interrupt appends in the ITLatch8 register
[6]	**ITFromLatch7** 0: Inactive 1: At least one interrupt appends in the ITLatch7 register
[5]	Reserved
[4]	**ITFromLatch5** 0: Inactive 1: At least one interrupt appends in the ITLatch5 register
[3]	**ITFromLatch4** 0: Inactive 1: At least one interrupt appends in the ITLatch4 register
[2]	**ITFromLatch3** 0: Inactive 1: At least one interrupt appends in the ITLatch3 register
[1]	**ITFromLatch2** 0: Inactive 1: At least one interrupt appends in the ITLatch2 register
[0]	**ITFromLatch1** 0: Inactive 1: At least one interrupt appends in the ITLatch1 register

ITLatchHier2 — Hierarchical interrupt

7	6	5	4	3	2	1	0
Reserved				ITFromLatch12	Reserved	ITFromLatch10	ITFromLatch9
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E61

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Hierarchical interrupts

[7:4]	Reserved
[3]	**ITFromLatch12** 0: Inactive 1: At least one interrupt appends in the ITLatch12 register
[2]	Reserved
[1]	**ITFromLatch10** 0: Inactive 1: At least one interrupt appends in the ITLatch10 register
[0]	**ITFromLatch9** 0: Inactive 1: At least one interrupt appends in the ITLatch9 register

ITLatchHier3 — Hierarchical interrupt

7	6	5	4	3	2	1	0
Reserved		ITFromLatch22	ITFromLatch21	ITFromLatch20	ITFromLatch19	Reserved	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0E62

Type: R

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: Hierarchical interrupts

[7:6]	Reserved
[5]	**ITFromLatch22** 0: Inactive 1: At least one interrupt appends in the ITLatch22 register
[4]	**ITFromLatch21** 0: Inactive 1: At least one interrupt appends in the ITLatch21 register
[3]	**ITFromLatch20** 0: Inactive 1: At least one interrupt appends in the ITLatch20 register
[2]	**ITFromLatch19** 0: Inactive 1: At least one interrupt appends in the ITLatch19 register
[1:0]	Reserved

4.4.12 RTC

Bank 0xF

SwitchOffStatus SwitchOffStatus

7	6	5	4	3	2	1	0
ThDB8500 SwOffCmd	PonKey1LongF	PORnVbat	Clk32kProt	WdogErr	BattOkProt	ThSDProt	SwOffCmd
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0F00

Type: R

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Stores switch off event

[7]	**ThDB8500SwOffCmd** 0: AB8500 has not switched off due to DB8500 / AP9500 thermal shutdown. 1: AB8500 has switched off due to DB8500 / AP9500 thermal shutdown.
[6]	**PonKey1LongF** 0: AB8500 has not switched off with a PonKey1 pressure longer than 10 s. 1: AB8500 has switched off with a PonKey1 pressure longer than 10 s.
[5]	**PornVbat** 0: AB8500 has not switched off due to a battery level lower than PornVbat threshold. 1: AB8500 has switched off due to a battery level lower than PornVbat threshold.
[4]	**Clk32kProt** 0: AB8500 has not switched off due to the non presence of 32 kHz clock. 1: AB8500 has switched off due to the non presence of 32 kHz clock.
[3]	**WdogErr** 0: AB8500 has not switched off due to primary watchdog has expired. 1: AB8500 has switched off due to primary watchdog has expired.
[2]	**BatOkProt** 0: AB8500 has not switched off due to a VbatA ball level lower than BattOk falling threshold. 1: AB8500 has switched off due to a VbatA ball level lower than BattOk falling threshold.
[1]	**ThSDProt** 0: AB8500 has not switched off due to Thermal protection activation. 1: AB8500 has switched off due to Thermal protection activation.
[0]	**SwOffCmd** 0: AB8500 has not switched off due to ‘Swoff’ bit programming. 1: AB8500 has switched off with ‘Swoff’ bit of STw4500Ctrl1 register.

CCConf CoulombCounterConfiguration

7	6	5	4	3	2	1	0
Reserved							CCPwrUpEna
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0F01

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Configuration of Coulomb counter

[7:1]	Reserved
[0]	**CCPwrUpEna** Note: Coulomb Counter always disable in PwrOff mode. 0: Disable Coulomb Counter 1: Enable Coulomb Counter

RTCReadRequest RTCReadRequest

7	6	5	4	3	2	1	0
Reserved						RtcWrite	RtcRead
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0F02

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: RTC feature management

[7:2]	Reserved
[1]	**RtcWrite** 0: No RC data transfer is required 1: RTC data write transfer is required. Cleared upon data transfer in watchtime register is done
[0]	**RtcRead** 0: No RTC data transfer is required 1: RTC data read transfer is required. Cleared upon data transfer in watchtime register is done

Watchtime registers

WatchtimeSecLow — WatchtimeSecLow

7	6	5	4	3	2	1	0
WatchtimeSec[7:0]							
R/W							

Address: BaseAddress: 0x0F03

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Watch time second value - 8 LSB

[7:0]	**WatchtimeSec[7:0]** Watchtime second data (8 LSB)

WatchtimeSecHigh — WatchtimeSecHigh

7	6	5	4	3	2	1	0
WatchtimeSec[15:8]							
R/W							

Address: BaseAddress: 0x0F04

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Watch time second value - 8 MSB

[7:0]	**WatchtimeSec[15:8]** Watchtime second data (8 MSB)

WatchtimeMinLow — Watchtime min low

7	6	5	4	3	2	1	0
WatchtimeMin[7:0]							
R/W							

Address: BaseAddress: 0x0F05

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Watch time minute value - 8 LSB

[7:0]	**WatchtimeMin[7:0]** Watchtime minute data (8 LSB**)**

WatchtimeMinMid — Watchtime Minutes mid

7	6	5	4	3	2	1	0
WatchtimeMin[15:8]							
R/W							

Address: BaseAddress: 0x0F06

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Watch time minute value - intermediate bits

[7:0]	**WatchtimeMin[15:8]** Watchtime minute data

WatchtimeMinHigh — Watchtime Minutes High

7	6	5	4	3	2	1	0
WatchtimeMin[23:16]							
R/W							

Address: BaseAddress: 0x0F07

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Watch time minute value - 8 MSB

[7:0]	**WatchtimeMin[23:16]** Watchtime minute data (8 MSB)

Alarm registers

AlarmMinLow — Alarm min low

7	6	5	4	3	2	1	0
AlarmMin[7:0]							
R/W							

Address: BaseAddress: 0x0F08

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Alarm minute value.

[7:0]	**AlarmMin[7:0] Alarm data** Alarm Minute data (8 LSB)

AlarmMinMid — Alarm min mid

7	6	5	4	3	2	1	0
AlarmMin[15:8]							
R/W							

Address: BaseAddress: 0x0F09

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Alarm minute value - intermediate bits.

[7:0]	**AlarmMin[15:8] Alarm data** Alarm Minute data

AlarmMinHigh — Alarm min high

7	6	5	4	3	2	1	0
AlarmMin[23:16]							
R/W							

Address: BaseAddress: 0x0F0A

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Alarm minute value - 8 MSB

[7:0]	**AlarmMin[23:16] Alarm data** Alarm Minute data (8 MSB)

RtcCtrl — RTC control

7	6	5	4	3	2	1	0
Reserved		BupChOffValid	BupChEna	BupPresent	RtcAlarmEna	Reserved	RtcStatusData
R/W	R/W	R/W	R/W	R/W	R/W		R/W

Address: BaseAddress: 0x0F0B

Type: R/W

Reset: 0x08 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: RTC and back up battery status

[7:6]	Reserved
[5]	**BupChOffValid** 0: Current source to charge back up battery disabled in OFF mode 1: Current source to charge back up battery enabled in OFF mode
[4]	**BupChEna** 0: Backup charger is disabled 1: Backup charger is enabled
[3]	**BupPresent** 0: No backup battery connected 1: Backup battery connected
[2]	**RtcAlarmEna** 0: RTC alarm disabled 1: RTC alarm enabled
[1]	Reserved
[0]	**RtcStatusData** 0: Reset by PorRtc Set at 1 by software and then reset if RTC supply fails

RtcBackupChg — RTC backup chg

7	6	5	4	3	2	1	0
Reserved				BupIchSel[1:0]		BupVchSel[1:0]	
				R/W		R/W	

Address: BaseAddress: 0x0F0C

Type: R/W

Reset: 0x04 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Back up battery management

[7:4]	Reserved
[3:2]	**BupIchSel[1:0]** Define the current to charge the back up battery 00: 50 µA 01: 150 µA 10: 300 µA 11: 700 µA
[1:0]	**BupVchSel[1:0]** Define the voltage at which the back up battery is charged 00: 2.5 V 01: 2.6 V 10: 2.8 V 11: 3.1 V

RtcForceBackup — RTC force backup

7	6	5	4	3	2	1	0
Reserved							ForceBackup
							R/W

Address: BaseAddress: 0x0F0D

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: Back Up supply management

[7:1]	Reserved
[0]	**ForceBackup** 0: Inactive 1: Force backup battery as supply for RTC block

RtcCalibration — RTC Calibration

7	6	5	4	3	2	1	0
RtcCalibration[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x0F0E

Type: R/W

Reset: 0x00 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: RTC derivation compensation

[7:0]	**RtcCalibration[7]** Sign bit **RtcCalibration[6:0]** Watchtime calibration register (correction every 60 s). 1 LSB = 30.5 µs which corresponds to 0.5 ppm of 32 kHz clock

RtcSwitchStatus — RtcSwitchStatus

7	6	5	4	3	2	1	0
Reserved					Xtal32kOK	32kHzStatus[1:0]	
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x0F0F

Type: R

Reset: 0x04 at first ON state, then “unchanged”, reset only by PornVrtc internal signal

Description: 32 kHz clock signal status

[7:3]	Reserved
[2]	**Xtal32kOK** 0: Xtal 32 kHz oscillator is stopped 1: Xtal 32 kHz oscillator is running
[1:0]	**32kHzStatus[1:0]** 00: No clock available (only possible in test mode) 01: Internal 32 kHz RC oscillator selected 10: Internal 32 kHz Xtal oscillator selected (when Xtal selected, internal RC oscillator is turned off)

4.4.13 GPIO's

GpioSel1 GpioSel1

7	6	5	4	3	2	1	0
Gpio8Sel	Gpio7Sel	Gpio6Sel	Reserved	Gpio4Sel	Gpio3Sel	Gpio2Sel	Gpio1Sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1000

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO ball control

[7]	**Gpio8Sel** 0: Ball is used as YCbCr2 1: Ball is used as GPIO8
[6]	**Gpio7Sel** 0: Ball is used as YCbCr1 1: Ball is used as GPIO7
[5]	**Gpio6Sel** 0: Ball is used as YCbCr0 1: Ball is used as GPIO6
[4]	Reserved
[3]	**Gpio4Sel** 0: Ball is used as SysClkReq6 1: Ball is used as GPIO4
[2]	**Gpio3Sel** 0: Ball is used as SysClkReq4 1: Ball is used as GPIO3
[1]	**Gpio2Sel** 0: Ball is used as SysClkReq3 1: Ball is used as GPIO2
[0]	**Gpio1Sel** 0: Ball is used as SysClkReq2 1: Ball is used as GPIO1

GpioSel2 GpioSel2

7	6	5	4	3	2	1	0
Gpio16Sel	Gpio15Sel	Gpio14Sel	Gpio13Sel	Gpio12Sel	Gpio11Sel	Gpio10Sel	Gpio9Sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1001

Type: R/W

Reset: 0x1E (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO ball control

[7]	**Gpio16Sel** 0: Ball is used as PWMOut3 1: Ball is used as GPIO16
[6]	**Gpio15Sel** 0: Ball is used as PWMOut2 1: Ball is used as GPIO15
[5]	**Gpio14Sel** 0: Ball is used as PWMOut1 1: Ball is used as GPIO14
[4]	**Gpio13Sel** 0: Ball is used as alternate function (*AlternatFunction* register) 1: Ball is used as GPIO13
[3]	**Gpio12Sel** 0: Ball is used as alternate function (*AlternatFunction* register) 1: Ball is used as GPIO12
[2]	**Gpio11Sel** 0: Ball is used as alternate function (*AlternatFunction* register) 1: Ball is used as GPIO11
[1]	**Gpio10Sel** 0: Ball is used as alternate function (*AlternatFunction* register) 1: Ball is used as GPIO10
[0]	**Gpio9Sel** 0: Ball is used as YCbCr3 1: Ball is used as GPIO9

GpioSel3 GpioSel3

7	6	5	4	3	2	1	0
Gpio24Sel	Gpio23Sel	Gpio22Sel	Gpio21Sel	Reserved			Gpio17_18_19_20Sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1002

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO ball control

[7]	**Gpio24Sel** 0: Ball is used as SysClkReq7 1: Ball is used as GPIO24
[6]	**Gpio23Sel** 0: Ball is used as UsbUiccSe0 1: Ball is used as GPIO23
[5]	**Gpio22Sel** 0: Ball is used as UsbUiccData 1: Ball is used as GPIO22
[4]	**Gpio21Sel** 0: Ball is used as UsbUiccDir 1: Ball is used as GPIO21
[3:1]	Reserved
[0]	**Gpio17_18_19_20_Sel** (Gpio17 is multiplexed with AD_Data1, Gpio18 is multiplexed with DA_Data1, Gpio19 is multiplexed with Fsync1, Gpio20 is multiplexed with BitClk1) 0: Ball is used as AD_Data1, DA_Data1, Fsync1 and BitClk1 1: Ball is used as GPIO17, GPIO18, GPIO19 and GPIO20 Note: Use these balls as GPIO, ‘SwReset’ bit of *AudSwReset* register must be previously set to “1”.

GpioSel4 GpioSel4

7	6	5	4	3	2	1	0
Gpio32Sel	Gpio31Sel	Gpio30Sel	Gpio29Sel	Gpio28Sel	Gpio27Sel	Reserved	Gpio25Sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1003

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO ball control

[7]	**Gpio32Sel** 0: Select Dmic56Dat 1: Select GPIO32
[6]	**Gpio31Sel** 0: Select Dmic56Clk 1: Select GPIO31
[5]	**Gpio30Sel** 0: Select Dmic34Dat 1: Select GPIO30
[4]	**Gpio29Sel** 0: Select Dmic34Clk 1: Select GPIO29
[3]	**Gpio28Sel** 0: Select Dmic12Dat 1: Select GPIO28
[2]	**Gpio27Sel** 0: Select Dmic12Clk 1: Select GPIO27
[1]	Reserved
[0]	**Gpio25Sel** 0: Ball is used as SysClkReq8 1: Ball is used as GPIO25

GpioSel5 GpioSel5

7	6	5	4	3	2	1	0
Gpio40Sel	Gpio39Sel	Gpio38Sel	Gpio37Sel	Gpio36Sel	Reserved	Gpio34Sel	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1004

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO ball control

[7]	**Gpio40Sel** 0: Ball is used as ModScl 1: Ball is used as GPIO40
[6]	**Gpio39Sel** 0: Ball is used as ApeSpiDin 1: Ball is used as GPIO39
[5]	**Gpio38Sel** 0: Ball is used as ApeSpiDout 1: Ball is used as GPIO38
[4]	**Gpio37Sel** 0: Ball is used as ApeSpiCSn 1: Ball is used as GPIO37
[3]	**Gpio36Sel** 0: Ball is used as ApeSpiClk 1: Ball is used as GPIO36
[2]	Reserved
[1]	**Gpio34Sel** 0: Ball is used as ExtCPEna (active high) 1: Ball is used as GPIO34
[0]	Reserved

GpioSel6 GpioSel6

7	6	5	4	3	2	1	0
Reserved						Gpio42Sel	Gpio41Sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1005

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO ball control

[7:2]	Reserved
[1]	**Gpio42Sel** 0: Ball is used as SysClkReq5 1: Ball is used as GPIO42
[0]	**Gpio41Sel** 0: Ball is used as ModSda 1: Ball is used as GPIO41

GpioDir1 GpioDir1

7	6	5	4	3	2	1	0
Gpio8Dir	Gpio7Dir	Gpio6Dir	Reserved	Gpio4Dir	Gpio3Dir	Gpio2Dir	Gpio1Dir
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1010

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Direction control

[7]	**Gpio8Dir** 0: GPIO8 direction is input 1: GPIO8 direction is output
[6]	**Gpio7Dir** 0: GPIO7 direction is input 1: GPIO7 direction is output
[5]	**Gpio6Dir** 0: GPIO6 direction is input 1: GPIO6 direction is output
[4]	Reserved
[3]	**Gpio4Dir** 0: GPIO4 direction is input 1: GPIO4 direction is output
[2]	**Gpio3Dir** 0: GPIO3 direction is input 1: GPIO3 direction is output
[1]	**Gpio2Dir** 0: GPIO2 direction is input 1: GPIO2 direction is output
[0]	**Gpio1Dir** 0: GPIO1 direction is input 1: GPIO1 direction is output

GpioDir2 GpioDir2

7	6	5	4	3	2	1	0
Gpio16Dir	Gpio15Dir	Gpio14Dir	Gpio13Dir	Gpio12Dir	Gpio11Dir	Gpio10Dir	Gpio9Dir
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1011

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Direction control

[7]	**Gpio16Dir** 0: GPIO16 direction is input 1: GPIO16 direction is output
[6]	**Gpio15Dir** 0: GPIO15 direction is input 1: GPIO15 direction is output
[5]	**Gpio14Dir** 0: GPIO14 direction is input 1: GPIO14 direction is output
[4]	**Gpio13Dir** 0: GPIO13 direction is input 1: GPIO13 direction is output
[3]	**Gpio12Dir** 0: GPIO12 direction is input 1: GPIO12 direction is output
[2]	**Gpio11Dir** 0: GPIO11 direction is input 1: GPIO11 direction is output
[1]	**Gpio10Dir** 0: GPIO10 direction is input 1: GPIO10 direction is output
[0]	**Gpio9Dir** 0: GPIO9 direction is input 1: GPIO9 direction is output

GpioDir3 GpioDir3

7	6	5	4	3	2	1	0
Gpio24Dir	Gpio23Dir	Gpio22Dir	Gpio21Dir	Gpio20Dir	Gpio19Dir	Gpio18Dir	Gpio17Dir
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1012

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Direction control

[7]	**Gpio24Dir** 0: GPIO23 direction is input 1: GPIO23 direction is output
[6]	**Gpio23Dir** 0: GPIO23 direction is input 1: GPIO23 direction is output
[5]	**Gpio22Dir** 0: GPIO22 direction is input 1: GPIO22 direction is output
[4]	**Gpio21Dir** 0: GPIO21 direction is input 1: GPIO21 direction is output
[3]	**Gpio20Dir** 0: GPIO20 direction is input 1: GPIO20 direction is output
[2]	**Gpio19Dir** 0: GPIO19 direction is input 1: GPIO19 direction is output
[1]	**Gpio18Dir** 0: GPIO18 direction is input 1: GPIO18 direction is output
[0]	**Gpio17Dir** 0: GPIO17 direction is input 1: GPIO17 direction is output

GpioDir4 GpioDir4

7	6	5	4	3	2	1	0
Gpio32Dir	Gpio31Dir	Gpio30Dir	Gpio29Dir	Gpio28Dir	Gpio27Dir	Gpio26Dir	Gpio25Dir
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1013

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Direction control

[7]	**Gpio32Dir** 0: GPIO32 direction is input 1: GPIO32 direction is output
[6]	**Gpio31Dir** 0: GPIO31 direction is input 1: GPIO31 direction is output
[5]	**Gpio30Dir** 0: GPIO30 direction is input 1: GPIO30 direction is output
[4]	**Gpio29Dir** 0: GPIO29 direction is input 1: GPIO29 direction is output
[3]	**Gpio28Dir** 0: GPIO28 direction is input 1: GPIO28 direction is output
[2]	**Gpio27Dir** 0: GPIO27 direction is input 1: GPIO27 direction is output
[1]	**Gpio26Dir** 0: GPIO26 direction is input 1: GPIO26 direction is output
[0]	**Gpio25Dir** 0: GPIO25 direction is input 1: GPIO25 direction is output

GpioDir5 GpioDir5

7	6	5	4	3	2	1	0
Gpio40Dir	Gpio39Dir	Gpio38Dir	Gpio37Dir	Gpio36Dir	Gpio35Dir	Gpio34Dir	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1014

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Direction control

[7]	**Gpio40Dir** 0: GPIO40 direction is input 1: GPIO40 direction is output
[6]	**Gpio39Dir** 0: GPIO39 direction is input 1: GPIO39 direction is output
[5]	**Gpio38Dir** 0: GPIO38 direction is input 1: GPIO38 direction is output
[4]	**Gpio37Dir** 0: GPIO37 direction is input 1: GPIO37 direction is output
[3]	**Gpio36Dir** 0: GPIO36 direction is input 1: GPIO36 direction is output
[2]	**Gpio35Dir** 0: GPIO35 direction is input 1: GPIO35 direction is output
[1]	**Gpio34Dir** 0: GPIO34 direction is input 1: GPIO34 direction is output
[0]	Reserved

GpioDir6 GpioDir6

7	6	5	4	3	2	1	0
Reserved						Gpio42Dir	Gpio41Dir
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1015

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Direction control

[7:2]	Reserved
[1]	**Gpio42Dir** 0: GPIO42 direction is input 1: GPIO42 direction is output
[0]	**Gpio41Dir** 0: GPIO41 direction is input 1: GPIO41 direction is output

GpioOut1 GpioOut1

7	6	5	4	3	2	1	0
Gpio8Out	Gpio7Out	Gpio6Out	Reserved	Gpio4Out	Gpio3Out	Gpio2Out	Gpio1Out
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1020

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Output control

[7]	**Gpio8Out** 0: GPIO8 output = “0” 1: GPIO8 output = “1”
[6]	**Gpio7Out** 0: GPIO7 output = “0” 1: GPIO7 output = “1”
[5]	**Gpio6Out** 0: GPIO6 output = “0” 1: GPIO6 output = “1”
[4]	Reserved
[3]	**Gpio4Out** 0: GPIO4 output = “0” 1: GPIO4 output = “1”
[2]	**Gpio3Out** 0: GPIO3 output = “0” 1: GPIO3 output = “1”
[1]	**Gpio2Out** 0: GPIO2 output = “0” 1: GPIO2 output = “1”
[0]	**Gpio1Out** 0: GPIO1 output = “0” 1: GPIO1 output = “1”

GpioOut2 GpioOut2

7	6	5	4	3	2	1	0
Gpio16Out	Gpio15Out	Gpio14Out	Gpio13Out	Gpio12Out	Gpio11Out	Gpio10Out	Gpio9Out
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1021

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Output control

[7]	**Gpio16Out** 0: GPIO16 output = “0” 1: GPIO16 output = “1”
[6]	**Gpio15Out** 0: GPIO15 output = “0” 1: GPIO15 output = “1”
[5]	**Gpio14Out** 0: GPIO14 output = “0” 1: GPIO14 output = “1”
[4]	**Gpio13Out** 0: GPIO13 output = “0” 1: GPIO13 output = “1”
[3]	**Gpio12Out** 0: GPIO12 output = “0” 1: GPIO12 output = “1”
[2]	**Gpio11Out** 0: GPIO11 output = “0” 1: GPIO11 output = “1”
[1]	**Gpio10Out** 0: GPIO10 output = “0” 1: GPIO10 output = “1”
[0]	**Gpio9Out** 0: GPIO9 output = “0” 1: GPIO9 output = “1”

GpioOut3 GpioOut3

7	6	5	4	3	2	1	0
Gpio24Out	Gpio23Out	Gpio22Out	Gpio21Out	Gpio20Out	Gpio19Out	Gpio18Out	Gpio17Out
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1022

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Output control

[7]	**Gpio24Out** 0: GPIO24 output = “0” 1: GPIO24 output = “1”
[6]	**Gpio23Out** 0: GPIO23 output = “0” 1: GPIO23 output = “1”
[5]	**Gpio22Out** 0: GPIO22 output = “0” 1: GPIO22 output = “1”
[4]	**Gpio21Out** 0: GPIO21 output = “0” 1: GPIO21 output = “1”
[3]	**Gpio20Out** 0: GPIO20 output = “0” 1: GPIO20 output = “1”
[2]	**Gpio19Out** 0: GPIO19 output = “0” 1: GPIO19 output = “1”
[1]	**Gpio18Out** 0: GPIO18 output = “0” 1: GPIO18 output = “1”
[0]	**Gpio17Out** 0: GPIO17 output = “0” 1: GPIO17 output = “1”

GpioOut4 GpioOut4

7	6	5	4	3	2	1	0
Gpio32Out	Gpio31Out	Gpio30Out	Gpio29Out	Gpio28Out	Gpio27Out	Gpio26Out	Gpio25Out
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1023

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Output control

[7]	**Gpio32Out** 0: GPIO32 output = “0” 1: GPIO32 output = “1”
[6]	**Gpio31Out** 0: GPIO31 output = “0” 1: GPIO31 output = “1”
[5]	**Gpio30Out** 0: GPIO30 output = “0” 1: GPIO30 output = “1”
[4]	**Gpio29Out** 0: GPIO29 output = “0” 1: GPIO29 output = “1”
[3]	**Gpio28Out** 0: GPIO28 output = “0” 1: GPIO28 output = “1”
[2]	**Gpio27Out** 0: GPIO27 output = “0” 1: GPIO27 output = “1”
[1]	**Gpio26Out** 0: GPIO26 output = “0” 1: GPIO26 output = “1”
[0]	**Gpio25Out** 0: GPIO25 output = “0” 1: GPIO25 output = “1”

GpioOut5 GpioOut5

7	6	5	4	3	2	1	0
Gpio40Out	Gpio39Out	Gpio38Out	Gpio37Out	Gpio36Out	Gpio35Out	Gpio34Out	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1024

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Output control

[7]	**Gpio40Out** 0: GPIO40 output = “0” 1: GPIO40 output = “1”
[6]	**Gpio39Out** 0: GPIO39 output = “0” 1: GPIO39 output = “1”
[5]	**Gpio38Out** 0: GPIO38 output = “0” 1: GPIO38 output = “1”
[4]	**Gpio37Out** 0: GPIO37 output = “0” 1: GPIO37 output = “1”
[3]	**Gpio36Out** 0: GPIO36 output = “0” 1: GPIO36 output = “1”
[2]	**Gpio35Out** 0: GPIO35 output = “0” 1: GPIO35 output = “1”
[1]	**Gpio34Out** 0: GPIO34 output = “0” 1: GPIO34 output = “1”
[0]	Reserved

GpioOut6 GpioOut6

7	6	5	4	3	2	1	0
Xtal32kHpLp[1:0]		Reserved				Gpio42Out	Gpio41Out
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1025

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Output control

[7:6]	**Xtal32kHpLp[1:0]** 0X: 32 kHz crystal oscillator is in Low power mode 10: 32 kHz crystal oscillator is in Mid power mode 11: 32 kHz crystal oscillator is in High power mode
[5:2]	Reserved
[1]	**Gpio42Out** 0: GPIO42 output = “0” 1: GPIO42 output = “1”
[0]	**Gpio41Out** 0: GPIO41 output = “0” 1: GPIO41 output = “1”

GpioPud1 GpioPud1

7	6	5	4	3	2	1	0
Gpio8Pudn	Gpio7Pudn	Gpio6Pudn	Reserved	Gpio4Pudn	Gpio3Pudn	Gpio2Pudn	Gpio1Pudn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1030

Type: R/W

Reset: 0xE0 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Pull-Down control

[7]	**Gpio8Pudn** 0: GPIO8 pull-down is enabled 1: GPIO8 pull-down is disabled
[6]	**Gpio7Pudn** 0: GPIO7 pull-down is enabled 1: GPIO7 pull-down is disabled
[5]	**Gpio6Pudn** 0: GPIO6 pull-down is enabled 1: GPIO6 pull-down is disabled
[4]	Reserved
[3]	**Gpio4Pudn** 0: GPIO4 pull-down is enabled 1: GPIO4 pull-down is disabled
[2]	**Gpio3Pudn** 0: GPIO3 pull-down is enabled 1: GPIO3 pull-down is disabled
[1]	**Gpio2Pudn** 0: GPIO2 pull-down is enabled 1: GPIO2 pull-down is disabled
[0]	**Gpio1Pudn** 0: GPIO1 pull-down is enabled 1: GPIO1 pull-down is disabled

GpioPud2 GpioPud2

7	6	5	4	3	2	1	0
Gpio16Pudn	Gpio15Pudn	Gpio14Pudn	Gpio13Pudn	Gpio12Pudn	Gpio11Pudn	Gpio10Pudn	Gpio9Pudn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1031

Type: R/W

Reset: 0x01 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Pull-Down control

[7]	**Gpio16Pudn** 0: GPIO16 pull-down is enabled 1: GPIO16 pull-down is disabled
[6]	**Gpio15Pudn** 0: GPIO15 pull-down is enabled 1: GPIO15 pull-down is disabled
[5]	**Gpio14Pudn** 0: GPIO14 pull-down is enabled 1: GPIO14 pull-down is disabled
[4]	**Gpio13Pudn** 0: GPIO13 pull-down is enabled 1: GPIO13 pull-down is disabled
[3]	**Gpio12Pudn** 0: GPIO12 pull-down is enabled 1: GPIO12 pull-down is disabled
[2]	**Gpio11Pudn** 0: GPIO11 pull-down is enabled 1: GPIO11 pull-down is disabled
[1]	**Gpio10Pudn** 0: GPIO10 pull-down is enabled 1: GPIO10 pull-down is disabled
[0]	**Gpio9Pudn** 0: GPIO9 pull-down is enabled 1: GPIO9 pull-down is disabled

GpioPud3 GpioPud3

7	6	5	4	3	2	1	0
Gpio24Pudn	Gpio23Pudn	Gpio22Pudn	Gpio21Pudn	Gpio20Pudn	Gpio19Pudn	Gpio18Pudn	Gpio17Pudn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1032

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Pull-Down control

[7]	**Gpio24Pudn** 0: GPIO24 pull-down is enabled 1: GPIO24 pull-down is disabled
[6]	**Gpio23Pudn** 0: GPIO23 pull-down is enabled 1: GPIO23 pull-down is disabled
[5]	**Gpio22Pudn** 0: GPIO22 pull-down is enabled 1: GPIO22 pull-down is disabled
[4]	**Gpio21Pudn** 0: GPIO21 pull-down is enabled 1: GPIO21 pull-down is disabled
[3]	**Gpio20Pudn** 0: GPIO20 pull-down is enabled 1: GPIO20 pull-down is disabled
[2]	**Gpio19Pudn** 0: GPIO19 pull-down is enabled 1: GPIO19 pull-down is disabled
[1]	**Gpio18Pudn** 0: GPIO18 pull-down is enabled 1: GPIO18 pull-down is disabled
[0]	**Gpio17Pudn** 0: GPIO17 pull-down is enabled 1: GPIO17 pull-down is disabled

GpioPud4 GpioPud4

7	6	5	4	3	2	1	0
Gpio32Pudn	Gpio31Pudn	Gpio30Pudn	Gpio29Pudn	Gpio28Pudn	Gpio27Pudn	Gpio26Pudn	Gpio25Pudn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1033

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Pull-Down control

[7]	**Gpio32Pudn** 0: GPIO32 pull-down is enabled 1: GPIO32 pull-down is disabled
[6]	**Gpio31Pudn** 0: GPIO31 pull-down is enabled 1: GPIO31 pull-down is disabled
[5]	**Gpio30Pudn** 0: GPIO30 pull-down is enabled 1: GPIO30 pull-down is disabled
[4]	**Gpio29Pudn** 0: GPIO29 pull-down is enabled 1: GPIO29 pull-down is disabled
[3]	**Gpio28Pudn** 0: GPIO28 pull-down is enabled 1: GPIO28 pull-down is disabled
[2]	**Gpio27Pudn** 0: GPIO27 pull-down is enabled 1: GPIO27 pull-down is disabled
[1]	**Gpio26Pudn** 0: GPIO26 pull-down is enabled 1: GPIO26 pull-down is disabled
[0]	**Gpio25Pudn** 0: GPIO25 pull-down is enabled 1: GPIO25 pull-down is disabled

GpioPud5 GpioPud5

7	6	5	4	3	2	1	0
Gpio40Pupn	Gpio39Pudn	Gpio38Pudn	Gpio37Pudn	Gpio36Pudn	Gpio35Pudn	Gpio34Pudn	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1034

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Pull-Up and Pull-Down control

[7]	**Gpio40Pupn** 0: GPIO40 pull-up is enabled 1: GPIO40 pull-up is disabled
[6]	**Gpio39Pudn** 0: GPIO39 pull-down is enabled 1: GPIO39 pull-down is disabled
[5]	**Gpio38Pudn** 0: GPIO38 pull-down is enabled 1: GPIO38 pull-down is disabled
[4]	**Gpio37Pudn** 0: GPIO37 pull-down is enabled 1: GPIO37 pull-down is disabled
[3]	**Gpio36Pudn** 0: GPIO36 pull-down is enabled 1: GPIO36 pull-down is disabled
[2]	**Gpio35Pudn** 0: GPIO35 pull-down is enabled 1: GPIO35 pull-down is disabled
[1]	**Gpio34Pudn** 0: GPIO34 pull-down is enabled 1: GPIO34 pull-down is disabled
[0]	Reserved

GpioPud6 GpioPud6

7	6	5	4	3	2	1	0
BattOkSelPudn	Reserved					Gpio42Pudn	Gpio41Pupn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1035

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Pull-Up and Pull-Down control

[7]	**BattOkSelPudn** 0: BattOkSel ball pull-up is enabled 1: BattOkSel ball pull-up is disabled Note: In an application where BatOkSel is connected to ground, to reduce AB8500 current consumption in deep sleep mode, this pull-up must be disabled
[6:2]	Reserved
[1]	**Gpio42Pudn** 0: GPIO42 pull-down is enabled 1: GPIO42 pull-down is disabled
[0]	**Gpio41Pupn** 0: GPIO41 pull-up is enabled 1: GPIO41 pull-up is disabled

GpioIn1 GpioIn1

7	6	5	4	3	2	1	0
Gpio8In	Gpio7In	Gpio6In	Reserved	Gpio4In	Gpio3In	Gpio2In	Gpio1In
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x1040

Type: R

Reset: 0xXX

Description: GPIO Input control

[7]	**Gpio8In** 0: GPIO8 input = “0” 1: GPIO8 input = “1”
[6]	**Gpio7In** 0: GPIO7 input = “0” 1: GPIO7 input = “1”
[5]	**Gpio6In** 0: GPIO6 input = “0” 1: GPIO6 input = “1”
[4]	Reserved
[3]	**Gpio4In** 0: GPIO4 input = “0” 1: GPIO4 input = “1”
[2]	**Gpio3In** 0: GPIO3 input = “0” 1: GPIO3 input = “1”
[1]	**Gpio2In** 0: GPIO2 input = “0” 1: GPIO2 input = “1”
[0]	**Gpio1In** 0: GPIO1 input = “0” 1: GPIO1 input = “1”

GpioIn2 GpioIn2

7	6	5	4	3	2	1	0
Gpio16In	Gpio15In	Gpio14In	Gpio13In	Gpio12In	Gpio11In	Gpio10In	Gpio9In
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x1041

Type: R

Reset: 0xXX

Description: GPIO Input control

[7]	**Gpio16In** 0: GPIO16 input = “0” 1: GPIO16 input = “1”
[6]	**Gpio15In** 0: GPIO15 input = “0” 1: GPIO15 input = “1”
[5]	**Gpio14In** 0: GPIO14 input = “0” 1: GPIO14 input = “1”
[4]	**Gpio13In** 0: GPIO13 input = “0” 1: GPIO13 input = “1”
[3]	**Gpio12In** 0: GPIO12 input = “0” 1: GPIO12 input = “1”
[2]	**Gpio11In** 0: GPIO11 input = “0” 1: GPIO11 input = “1”
[1]	**Gpio10In** 0: GPIO10 input = “0” 1: GPIO10 input = “1”
[0]	**Gpio9In** 0: GPIO9 input = “0” 1: GPIO9 input = “1”

GpioIn3 GpioIn3

7	6	5	4	3	2	1	0
Gpio24In	Gpio23In	Gpio22In	Gpio21In	Gpio20In	Gpio19In	Gpio18In	Gpio17In
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x1042

Type: R

Reset: 0xXX

Description: GPIO Input control

[7]	**Gpio24In** 0: GPIO24 Input = “0” 1: GPIO24 Input = “1”
[6]	**Gpio23In** 0: GPIO23 Input = “0” 1: GPIO23 Input = “1”
[5]	**Gpio22In** 0: GPIO22 Input = “0” 1: GPIO22 Input = “1”
[4]	**Gpio21In** 0: GPIO21 Input = “0” 1: GPIO21 Input = “1”
[3]	**Gpio20In** 0: GPIO20 Input = “0” 1: GPIO20 Input = “1”
[2]	**Gpio19In** 0: GPIO19 Input = “0” 1: GPIO19 Input = “1”
[1]	**Gpio18In** 0: GPIO18 Input = “0” 1: GPIO18 Input = “1”
[0]	**Gpio17In** 0: GPIO17 Input = “0” 1: GPIO17 Input = “1”

GpioIn4 GpioIn4

7	6	5	4	3	2	1	0
Gpio32In	Gpio31In	Gpio30In	Gpio29In	Gpio28In	Gpio27In	Gpio26In	Gpio25In
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x1043

Type: R

Reset: 0xXX

Description: GPIO Input control

[7]	**Gpio32In** 0: GPIO32 Input = “0” 1: GPIO32 Input = “1”
[6]	**Gpio31In** 0: GPIO31 Input = “0” 1: GPIO31 Input = “1”
[5]	**Gpio30In** 0: GPIO30 Input = “0” 1: GPIO30 Input = “1”
[4]	**Gpio29In** 0: GPIO29 Input = “0” 1: GPIO29 Input = “1”
[3]	**Gpio28In** 0: GPIO28 Input = “0” 1: GPIO28 Input = “1”
[2]	**Gpio27In** 0: GPIO27 Input = “0” 1: GPIO27 Input = “1”
[1]	**Gpio26In** 0: GPIO26 Input = “0” 1: GPIO26 Input = “1”
[0]	**Gpio25In** 0: GPIO25 Input = “0” 1: GPIO25 Input = “1”

GpioIn5 GpioIn5

7	6	5	4	3	2	1	0
Gpio40In	Gpio39In	Gpio38In	Gpio37In	Gpio36In	Gpio35In	Gpio34In	Reserved
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x1044

Type: R

Reset: 0xXX

Description: GPIO Input control

[7]	**Gpio40In** 0: GPIO40 Input = “0” 1: GPIO40 Input = “1”
[6]	**Gpio39In** 0: GPIO39 Input = “0” 1: GPIO39 Input = “1”
[5]	**Gpio38In** 0: GPIO38 Input = “0” 1: GPIO38 Input = “1”
[4]	**Gpio37In** 0: GPIO37 Input = “0” 1: GPIO37 Input = “1”
[3]	**Gpio36In** 0: GPIO36 Input = “0” 1: GPIO36 Input = “1”
[2]	**Gpio35In** 0: GPIO35 Input = “0” 1: GPIO35 Input = “1”
[1]	**Gpio34In** 0: GPIO34 Input = “0” 1: GPIO34 Input = “1”
[0]	Reserved

GpioIn6 GpioIn6

7	6	5	4	3	2	1	0
Reserved						Gpio42In	Gpio41In
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x1045

Type: R

Reset: 0xXX

Description: GPIO Input control

[7:2]	Reserved
[1]	**Gpio42In** 0: GPIO42 Input = “0” 1: GPIO42 Input = “1”
[0]	**Gpio41In** 0: GPIO41 Input = “0” 1: GPIO41 Input = “1”

AlternatFunction AlternatFunction

7	6	5	4	3	2	1	0
Reserved			Ycbcr7I2cTrig2UsbVdat[1:0]		Ycbcr6I2cTrig1	Ycbcr5UsbUiccPd	Ycbcr4HiqClkEna
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1050

Type: R/W

Reset: 0x02 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: GPIO Alternate function control

[7:5]	Reserved
[4:3]	**YcbCr7I2cTrig2UsbVdat[1:0]** 00: Select YcbCr7 function on ball Gpio13 01: Select I2cTrig2 function on ball Gpio13 10 or 11: Select USBVdat on ball Gpio13 (0: indicates 100 mA, 1: indicates 500 mA)
[2]	**YcbCr6I2cTrig1** 0: Select YcbCr6 function on ball Gpio12 1: Select I2cTrig1 function on ball Gpio12
[1]	**YcbCr5UsbUiccPd** 0: Select YcbCr5 function on ball Gpio11 1: Select UsbUiccPd function on ball Gpio11
[0]	**YcbCr4HiqClkEna** 0: Select YcbCr4 function on ball Gpio10 1: Select HiqClkEna function on ball Gpio10

4.4.14 PWMOut generators

PWMOutCtrl1 **PWMOutCtrl1**

7	6	5	4	3	2	1	0
DutyPWMOut1[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1060

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: PWMOut1 management

[7:0]	**DutyPWMOut1[7:0]** Defined, with 'DutyPWMOut1[9:8]' bits, PWMOut1 duty cycle (from 1 to 1024)

PWMOutCtrl2 PWMOutCtrl2

7	6	5	4	3	2	1	0
FreqPWMOut1[3:0]				Reserved		DutyPWMOut1[9:8]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1061

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: PWMOut1 management

[7:4]	**FreqPWMOut1[3:0]** 0000: 293 Hz 0001: 302 Hz 0010: 312 Hz 0011: 323 Hz 0100: 334 Hz 0101: 347 Hz 0110: 360 Hz 0111: 375 Hz 1000: 390 Hz 1001: 407 Hz 1010: 426 Hz 1011: 446 Hz 1100: 468 Hz 1101: 493 Hz 1110: 520 Hz 1111: 551 Hz
[3:2]	Reserved
[1:0]	**DutyPWMOut1[9:8]** DutyPWMOut1[9:0] defined PWMOut1 duty cycle (from 1 to 1024) All bits = 0: 1/1024 then step of 1/1024 up to all bits = 1: 1024/1024

Note: DutyPWMOut[9:0]: 0000000000 = 1/1024; 0000000001 = 2/1024;.....; 1111111110 = 1023/1024; 1111111111 = 1024/1024.

PWMOutCtrl3 PWMOutCtrl3

7	6	5	4	3	2	1	0
DutyPWMOut2[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1062

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: PWMOut2 management

[7:0]	**DutyPWMOut2[7:0]** Defined, with 'DutyPWMOut2[9:8]' bits, PWMOut2 duty cycle (from 1 to 1024)

PWMOutCtrl4 PWMOutCtrl4

7	6	5	4	3	2	1	0
FreqPWMOut2[3:0]				Reserved		DutyPWMOut2[9:8]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1063

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: PWMOut2 management

[7:4]	**FreqPWMOut2[3:0]** 0000: 293 Hz 0001: 302 Hz 0010: 312 Hz 0011: 323 Hz 0100: 334 Hz 0101: 347 Hz 0110: 360 Hz 0111: 375 Hz 1000: 390 Hz 1001: 407 Hz 1010: 426 Hz 1011: 446 Hz 1100: 468 Hz 1101: 493 Hz 1110: 520 Hz 1111: 551 Hz
[3:2]	Reserved
[1:0]	**DutyPWMOut2[9:8]** DutyPWMOut2[9:0] defined PWMOut2 duty cycle (from 1 to 1024)

Note: DutyPWMOut[9:0]: 0000000000 = 1/1024; 0000000001 = 2/1024;.....; 1111111110 = 1023/1024; 1111111111 = 1024/1024.

PWMOutCtrl5 PWMOutCtrl5

7	6	5	4	3	2	1	0
DutyPWMOut3[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1064

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: PWMOut3 management

[7:0]	**DutyPWMOut3[7:0]** Defined, with 'DutyPWMOut3[9:8]' bits, PWMOut3 duty cycle (from 1 to 1024)

PWMOutCtrl6 PWMOutCtrl6

7	6	5	4	3	2	1	0
FreqPWMOut3[3:0]				Reserved		DutyPWMOut3[9:8]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1065

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: PWMOut3 management

[7:4]	**FreqPWMOut3[3:0]** 0000: 293 Hz 0001: 302 Hz 0010: 312 Hz 0011: 323 Hz 0100: 334 Hz 0101: 347 Hz 0110: 360 Hz 0111: 375 Hz 1000: 390 Hz 1001: 407 Hz 1010: 426 Hz 1011: 446 Hz 1100: 468 Hz 1101: 493 Hz 1110: 520 Hz 1111: 551 Hz
[3:2]	Reserved
[1:0]	**DutyPWMOut3[9:8]** DutyPWMOut3[9:0] defined PWMOut3 duty cycle (from 1 to 1024)

Note: DutyPWMOut[9:0]: 0000000000 = 1/1024; 0000000001 = 2/1024;.....; 1111111110 = 1023/1024; 1111111111 = 1024/1024.

PWMOutCtrl7 PWMOutCtrl7

7	6	5	4	3	2	1	0
Reserved					EnaPWMOut3	EnaPWMOut2	EnaPWMOut1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1066

Type: R/W

Reset: 0x00 (StdRegRstn, DigPORn, SwitchOffRstn)

Description: PWM generator enabling

[7:3]	Reserved
[2]	**EnaPWMOut3** 0: Disable PWMOut3 generator 1: Enable PWMOut3 generator
[1]	**EnaPWMOut2** 0: Disable PWMOut2 generator 1: Enable PWMOut2 generator
[0]	**EnaPWMOut1** 0: Disable PWMOut1 generator 1: Enable PWMOut1 generator

I2CPadCtrl I2CPadCtrl

7	6	5	4	3	2	1	0
Reserved				ApeSdaPup EnaN	ApeSclPup EnaN	ModSdaPup EnaN	ModSclPup EnaN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: BaseAddress: 0x1067

Type: R/W

Reset: 0x00 (DigPORn, SwitchOffRstn)

Description: I2C interface pull-up control

[7:4]	Reserved
[3]	**ApeSdaPupEnaN** 0: Enable internal pull-up 1: Disable internal pull-up
[2]	**ApeSclPupEnaN** 0: Enable internal pull-up 1: Disable internal pull-up
[1]	**ModSdaPupEnaN** 0: Enable internal pull-up 1: Disable internal pull-up
[0]	**ModSclPupEnaN** 0: Enable internal pull-up 1: Disable internal pull-up

AB8500rev I2CPadCtrl

7	6	5	4	3	2	1	0
FullMask[3:0]				MetalFix[3:0]			
R	R	R	R	R	R	R	R

Address: BaseAddress: 0x1080

Type: R

Reset: 0x30 (cut 3.0)

Description: AB8500 revision version

[7:4]	**FullMask[3:0]** Full mask set revision
[3:0]	**MetalFix[3:0]** Partial mask set revision

4.4.15 Registers for development activity

This information is not available in the public domain.

4.4.16 Bank 12 registers

This information is not available in the public domain

4.4.17 Registers for ADC calibration

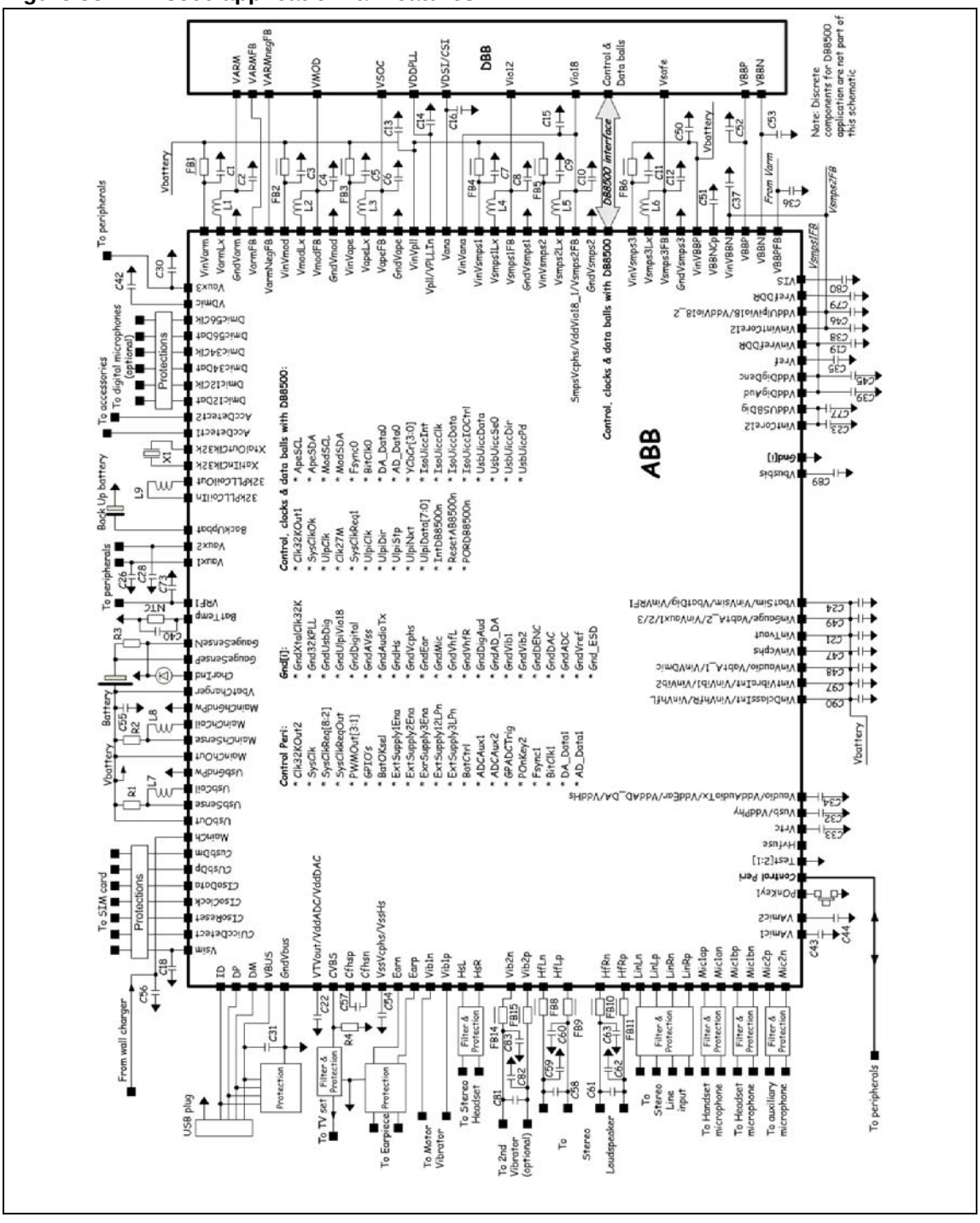
These read registers are from address 0x150F up to 0x1515, see*Table 11: ADC calibration* in *Section 3.9: ADC general purpose* for details.

4.4.18 OTP bit configuration

This information is not available in the public domain.

5 Typical application

Figure 38. AB8500 application: all features



List of material / All features

Table 19. AB8500 application / All features

Components	Value	Reference	Supplier	Comments
Power management				
DB8500 / AP9500 & I/O's supplies (Varm, Vmod, Vape, Vsafe, Vana, Vpll, Vio12, Vio18, DB8500 / AP9500 biasing)				
C1, C3, C5, C7, C9, C11	10 µF	GRM188R60J106ME47D GRM155R60J106M C1608X5R0J106M	Murata Murata TDK	6.3 V
C2, C4, C6, C8, C10, C12	22 µF	GRM21BR60J226ME39 C2012X5R0J226MTJ	Murata TDK	6.3 V
C13, C15, C51	100 nF	GRM033R60J104ME19 C1005X5R1C104K	Murata TDK	
C14, C16, C36, C37, C50	1 µF or 2.2 µF	C1005X5R0J105K GRM155R60J225ME15D CM05X5R225K06AHN0	TDK Murata Kyocera	6.3 V 2.2 µF recommended on LDO outputs
C52	100 nF	GRM033R60J104ME19 C1005X5R1C104K	Murata TDK	100 nF close to AB8500 and 100 nF close to DB8500 / AP9500
C53	1 µF	C1005X5R0J105K	TDK	6.3 V
FB1, FB2, FB3, FB4, FB5, FB6	-	BLM18KG221SN1	Murata	Ferrite bead
L1, L2, L3, L4, L5	1 µH	LQM2HPN1R0MJC	Murata	
L6	1 µH	LQM21PN1R0MC0	Murata	
AB8500 interface supplies (VADC, VTVout, Vrtc), references (Vref, VIS), input supply decoupling, 32 kHz PLL and oscillator				
C21,C38, C45.	100 nF	GRM033R60J104ME19 C1005X5R1C104K	Murata TDK	
C22, C23, C33, C35, C80	1 µF or 2.2 µF	C1005X5R0J105K GRM155R60J225ME15D CM05X5R225K06AHN0	TDK Murata Kyocera	6.3 V 2.2 µF recommended on LDO outputs
L9	47 nH	LQG15HN47NJ02	Murata	
R4	75 Ω	CC0402 - 5%		63mW
X1	32.768 kHz	CC7V-T1A CX8V-T1A	Micro Crystal	
Peripheral supplies (VrefDDR, Vaux1, Vaux2, Vaux3, VRF1, Vsim)				
C19	100 nF	GRM033R60J104ME19 C1005X5R1C104K	Murata TDK	
C18, C24, C26, C28, C30, C73	1 µF or 2.2 µF	C1005X5R0J105K GRM155R60J225ME15D CM05X5R225K06AHN0	TDK Murata Kyocera	6.3 V 2.2 µF recommended on LDO outputs
C79	4.7 nF	C1005X5R1H472K	TDK	6.3 Vmin

Table 19. AB8500 application / All features (continued)

Components	Value	Reference	Supplier	Comments
Energy management				
Wall charger, USB charger, Coulomb counter				
C31	4.7 µF	GRM21BR61C475K C2012X5R1C475K	Murata TDK	16 V
C40	1 nF	GRM033R71E102K C1005X5R1H102K	Murata TDK	
C49	1 µF or 2.2 µF	C1005X5R0J105K GRM155R60J225ME15D CM05X5R225K06AHN0	TDK Murata Kyocera	6.3 V
C55	2.2 µF	GRM188R61A225KE34D	Murata	10 V
C56	4.7 µF	GRM21BR61E475KA12	Murata	25 V
R1, R2	68 mΩ	UCR01MVPFS0R68	Rhom	125 mW - 1005(0402)
R3	10 mΩ	PMR03EZPFU10L0	Rhom	250 mW - 1608(0603)
L7, L8	1 µH	CIG32W1R0MNE LQM2HPN1R0MJC CIG10W1R0MNC	Samsung Murata Samsung	Icharger up to 1.5 A Icharger up to 1 A Icharger up to 0.7 A
NTC	47 kΩ	NCP15WB473F03RC	Murata	B-Constant = 4050 - 1%
Audio				
Supplies (Vaudio, Vcphs, VAmic1, VAmic2, VDmic) and input decoupling				
C34	10 µF	GRM188R60J106ME47D GRM155R60J106M C1608X5R0J106M	Murata Murata TDK	6.3 V
C39	100 nF	GRM033R60J104ME19 C1005X5R1C104K	Murata TDK	
C42, C47, C48, C90, C97	1 µF or 2.2 µF	C1005X5R0J105K GRM155R60J225ME15D CM05X5R225K06AHN0	TDK Murata Kyocera	6.3 V
C43, C44	470 pF	GRM033R71C471KA01 C1005X5R1H471K	Murata TDK	
C54, C57	2.2 µF	GRM155R60J225ME15D CM05X5R225K06AHN0	TDK Kyocera	6.3 V
Stereo loudspeaker				
C58, C59, C60, C61, C62, C63	1 nF	GRM033R71E102K C1005X5R1H102K	Murata TDK	
FB8, FB9, FB10, FB11	-	BLM15PD121SN1	Murata	Ferrite bead
Vibrator				
C81, C82, C83	1 nF	GRM033R71E102K C1005X5R1H102K	Murata TDK	6.3 Vmin
FB14, FB15	-	BLM15PD121SN1	Murata	Ferrite bead

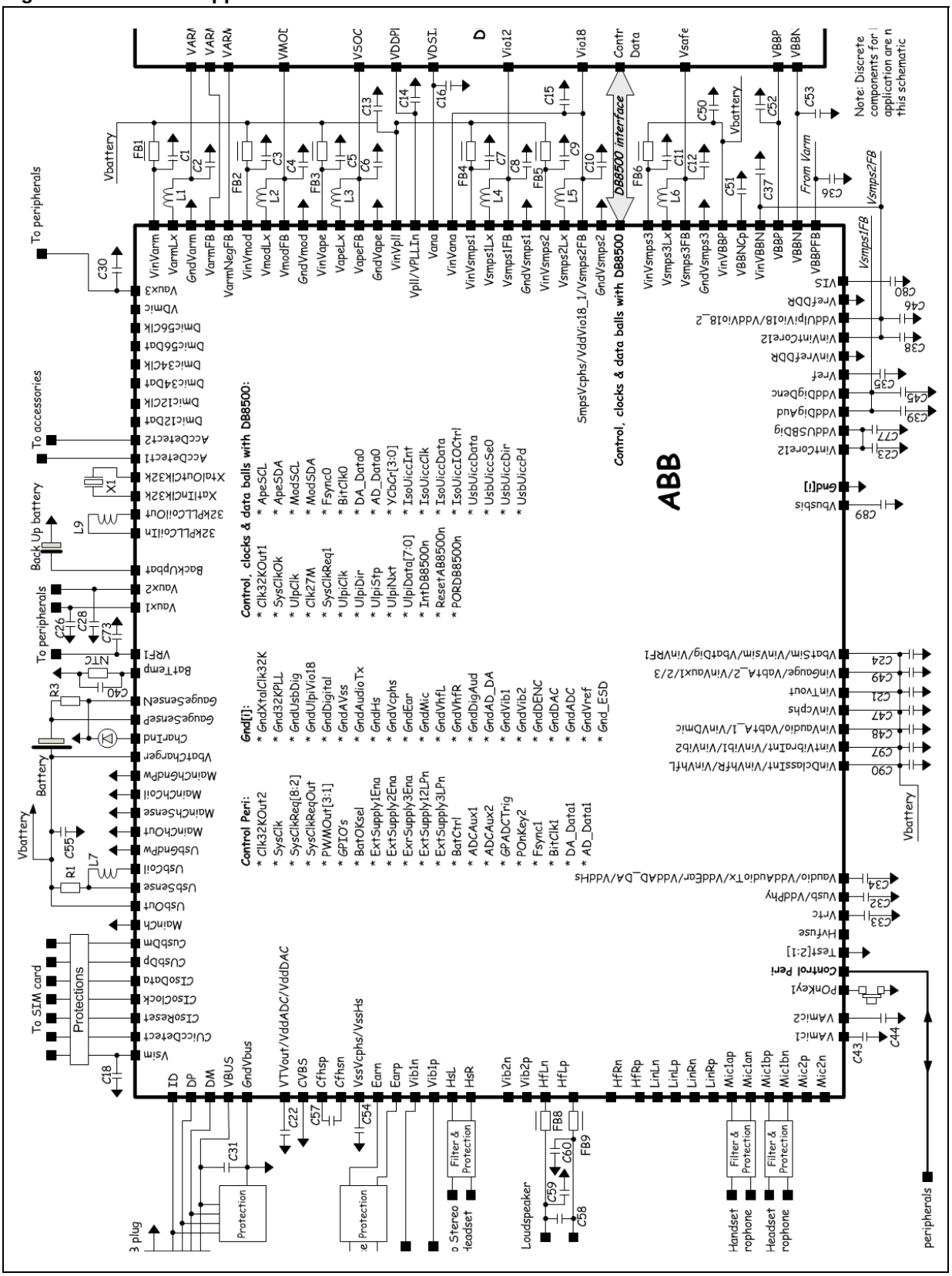
Table 19. AB8500 application / All features (continued)

Components	Value	Reference	Supplier	Comments
High Speed USB physical interface				
C32	1 µF or 2.2 µF	C1005X5R0J105K GRM155R60J225ME15D CM05X5R225K06AHN0	TDK Murata Kyocera	6.3 V
C89	4.7 µF	GRM188R61A475ME19D C1608X5R0J475K	Murata TDK	6.3 V
C46, C77	100 nF	GRM033R60J104ME19 C1005X5R1C104K	Murata TDK	16 V

Figure 39: Application with

- Main charger not used, only USB charger
- One loudpeaker (Mono mode)
- One Motor vibrator, second vibrator not used
- Analog handset and headset microphones, auxiliary microphone and digital microphone not used
- Stereo line input not used
- Tvout feature not used
- VrefDDR not used

Figure 39. AB8500 application: reduced set of features



5.1 Unused features

Table 20 provides the information about how to connect the balls when a feature is unused.

- N.C.: Left opened
- N.A.: Cannot be unused with DB8500 / AP9500.

Table 20. Ball connection if feature is unused

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
Control					
	General control				
C5	POnKey1	DI 100k PU	ON/OFF key pressure (active low)	N.A.	N.A.
C4	POnKey2	DI 100k PU	Additional power ON/OFF control (active low)	Vbat	Vbat
D2	ExtSupply1Ena	DO at high or low level depends on OTP settings	External Vio enable if used (or other external supply)	N.C.	N.C.
C2	ExtSupply2Ena		External Vcore (or other external supply) enable if used	N.C.	N.C.
E5	ExtSupply3Ena		External Buck boost (or other external supply) enable if used	N.C.	N.C.
J17	ExtSupply12LPn / ExtSupply12Clk		Clock / Low Power command (active low) for external supply 1&2 (Vio18 and Vcore or other ext. supply)	N.C.	N.C.
F13	ExtSupply3LPn / ExtSupply3Clk		Clock / Low Power command (active low) for external supply (buck boost or ext. supply)	N.C.	N.C.
	DB8500 / AP9500 control				
U10	ResetAB8500n	DI	AB8500 reset (active low)	N.A.	N.A.
U14	PORDB8500n	DO High Level	DB8500 / AP9500 reset (active low)	N.A.	N.A.
N17	IntDB8500n	DO High or Low Level(1)	AB8500 Interrupt to DB8500 / AP9500 (active low)	N.A.	N.A.
A17	ApeSpiClk/ GPIO36	DI	SPI clock / GPIO36	Gnd	To Gnd through a 100k
E15	ApeSpiCSn/ GPIO37	DI	SPI chip select / GPIO37	Vsmps2	Vsmps2
C17	ApeSpiDout/ GPIO38	DO HIZ	SPI data out / GPIO38	N.C.	N.C.
E16	ApeSpiDin/ GPIO39	DI	SPI data in / GPIO39	Gnd	To Gnd through a 100k

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
V19	ApeSCL	DI 350 Ω PU	Dedicated link - “PRCMU I2C clock” for DB8500 / AP9500 APE supplies voltage control	N.A.	N.A.
V20	ApeSDA	DI 350 Ω PU	Dedicated link “PRCMU I2C data” for DB8500 / AP9500 APE supplies voltage control	N.A.	N.A.
T19	ModSCL/ GPIO40	DI 350 Ω PU	I2C clock for DB8500 Modem supplies voltage selection and SIM register access / GPIO40	Vio18	N.C.
U19	ModSDA/ GPIO41	DI 350 Ω PU	I2C data for DB8500 Modem supplies voltage selection and SIM register access / GPIO41	Vio18	N.C.
C3	BatCtrl	AI 80k PU	Battery control / Battery type	To Gnd through a 220k	To Gnd through a 220k
	Clock management				
B10	XtalInClk32K		32 kHz internal oscillator input	N.A.	N.A.
C10	XtalOutClk32K		32 kHz internal oscillator output	N.A.	N.A.
C9	GndXtalClk32K		32 kHz internal oscillator ground	Gnd	Gnd
J16	Clk32kOut1	DO	32 k clock for DB8500 / AP9500	N.A.	N.A.
H17	Clk32kOut2	DO	32 k clock for peripheral devices	N.C.	N.C.
C7	32kPllCapFilter		Ulp clock PLL filter	N.C.	N.C.
A11	32kPllCoilOut		Ulp clock PLL coil connection	N.C.	N.C.
A10	32kPllCoilIn		Ulp clock PLL coil connection	N.C.	N.C.
C8	Gnd32kPll		Ulp clock PLL ground	Gnd	Gnd
T8	SysClkReq1	DI	System clock requested from DB8500 / AP9500.	N.A.	N.A.
T10	SysClkReq2 / GPIO1	DI	System clock requested from peripheral devices, or GPIO1	Gnd	To Gnd through a 100k
T9	SysClkReq3 / GPIO2	DI	System clock requested from peripheral devices, or GPIO2	Gnd	To Gnd through a 100k
U9	SysClkReq4 / GPIO3	DI	System clock requested from peripheral devices, or GPIO3	Gnd	To Gnd through a 100k
U2	SysClkReq5 / GPIO42	DI	System clock requested from peripheral devices or GPIO42	Gnd	To Gnd through a 100k
W2	SysClkReq6 / GPIO4	DI	System clock requested from peripheral devices or APE or GPIO4	Gnd	To Gnd through a 100k
T14	SysClkReq7 / GPIO24	DI	System clock request or GPIO24	Gnd	To Gnd through a 100k

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
R16	SysClkReq8 / GPIO25	DI	System clock request or GPIO25	Gnd	To Gnd through a 100k
V3	SysClkOk	DO High Level	System clock O.K signal to DB8500 / AP9500	N.A.	N.A.
Y2	SysClkReqOut	DO High Level	External RF clock generators enable	N.A.	N.A.
U17	HiqClkEna/ GPIO10	DI	External high quality clock enable or GPIO10	Gnd	N.C.
L16	SysClk	DI	System clock input square	N.A.	N.A.
F21	UlpClk	DI 50K PD	Ultra Low Power system clock output to DB8500 / AP9500	N.C.	N.C.
T16	Clk27M	DI 50K PD	27 MHz video clock to DB8500 / AP9500	N.C.	N.C.
Power management					
	AB8500 internal supplies				
E8	VbatDig		Digital positive supply	N.A.	N.A.
D1 W14	VbatA		Analog positive supply	N.A.	N.A.
R19	BattOkSel	DI	BattOk comparator threshold selection (for 2.3 V / 2.7V battery types)	N.A.	N.A.
K16 U6	VddVio18		1.8 V IO internal supply	N.A.	N.A.
K13	GndDigital		Digital grounds	Gnd	Gnd
J10 K9 L9 N12 U20	GndAvss		Analog grounds	Gnd	Gnd
J9 K10 N11	Gnd_ESD		ESD ring grounds	Gnd	Gnd
F9	Vrtc		32 kHz internal oscillator and RTC supply	N.A.	N.A.
W12	GndVref		1.8 V internal reference ground	Gnd	Gnd
E7	Vref		1.8 V internal reference	N.A.	N.A.
B16	VIS		Internal Supply	N.A.	N.A.
A8	VinVintCore12		Vint input power supply	N.A.	N.A.

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
B8	VintCore12		LDO output dedicated to supply AB8500 USB digital part	N.A.	N.A.
	DB8500 / AP9500 and I/O's supplies				
Y17 AA17	VinVape		Vape input power supply balls	N.A.	N.A.
Y16 AA16	VapeLx		Vape external coil connection balls	N.A.	N.A.
W16	VapeFB	Default output value	Vape feedback and DB8500 / AP9500 supply	N.A.	N.A.
Y15 AA15	GndVape		Vape ground balls	Gnd	Gnd
N20 N21	VinVarm		Varm input power supply balls	N.A.	N.A.
P20 P21	VarmLx		Varm external coil connection balls	N.A.	N.A.
T21	VarmFB	Default output value	Varm feedback and DB8500 / AP9500 supply	N.A.	N.A.
N19 P19	GndVarm		Varm ground balls	Gnd	Gnd
T20	VarmNegFB		Varm negative voltage feedback	Gnd	Gnd
Y11 AA11	VinVmod		Vmod input power supply balls	N.A.	N.A.
Y10 AA10	VmodLx		Vmod external coil connection balls	N.A.	N.A.
Y12	VmodFB	Default output value	Vmod feedbackX and DB8500 / AP9500 supply	N.A.	N.A.
Y9 AA9	GndVmod		Vmod ground balls	Gnd	Gnd
B1 C1	VinVsmps1		Vsmps1 input power supply balls	Vbat	Vbat
A2 A3	Vsmps1Lx		Vsmps1 external coil connection balls	N.C.	N.C.
B2	Vsmps1FB		Vsmps1 feedback and Vio12 supply	Gnd	Gnd
A4 B4	GndVsmps1		Vsmps1 ground balls	Gnd	Gnd

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
U1 V1	VinVsmps2		Vsmps2 input power supply balls	Vbat	Vbat
R1 T1	Vsmps2Lx		Vsmps2 external coil connection balls	N.C.	N.C.
V2	Vsmps2FB		Vsmps2 feedback and Vio18 supply	Gnd	Gnd
R2 T2	GndVsmps2		Vsmps2 ground balls	Gnd	Gnd
A5 B5	VinVsmps3		Vsmps3 input power supply ball	N.A.	N.A.
A6 B6	Vsmps3Lx		Vsmps3 external coil connection ball	N.A.	N.A.
C6	Vsmps3FB	Default output value	Vsmps3 feedback and DB8500 / AP9500 Vsafe supply	N.A.	N.A.
A7 B7	GndVsmps3		Vsmps3 ground ball	N.A.	N.A.
E1	VinVana		Vana input power supply	N.A.	N.A.
D3	Vana		Vana LDO output and DB8500 / AP9500 supply	N.A.	N.A.
A9	VinVpll		Vpll input power supply	N.A.	N.A.
B9	Vpll		Vpll LDO output for internal clock tree and DB8500 / AP9500 PLL	N.A.	N.A.
Y19	VinVBBP		VBBP input power supply	N.A.	N.A.
U15	VBBP	Varm	VBBP LDO output for DB8500 / AP9500 P-Type devices reverse/forward bias	N.A.	N.A.
U21	VBBPFB		Varm voltage feedback	N.A.	N.A.
T15	VBBN	GndA	VBBN LDO output for DB8500 / AP9500 N-Type devices reverse/forward bias	N.A.	N.A.
W19	VBBNCp		VBBNCp charge pump output	N.A.	N.A.
Y20	VinVBBN		VBBN input power supply	N.A.	N.A.
	Peripheral supplies				
Y21	VinVrefDDR		VrefDDR input supply	Gnd	Gnd
W21	VrefDDR		VrefDDR supply	Gnd	Gnd
C11	BackUpBat		Backup battery supply	Vbat	Vbat
E9	VinVRF1		VRF1 input power supply	N.A.	N.A.

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
B11	VRF1	Default output value	VRF1 LDO output for system clock oscillator	N.A.	N.A.
AA12	VinVaux1		Vaux1 input power supply	Vbat	Vbat
AA13	Vaux1	Software dependent	Vaux1 LDO output for peripheral devices	N.C.	N.C.
AA14	VinVaux2		Vaux2 input power supply	Vbat	Vbat
Y13	Vaux2	Software dependent	Vaux2 LDO output for peripheral devices	N.C.	N.C.
W11	VinVaux3		Vaux3 input power supply	Vbat	Vbat
W13	Vaux3	Software dependent	Vaux3 LDO output for peripheral devices	N.C.	N.C.
Energy management					
	Wall charger				
G21 H20 H21 J20	MainCh		Main charger cable	Gnd	Gnd
J21 K20 K21	MainChCoil		Main charger external coil connection balls	Gnd	Gnd
L20 L21 M21	MainChGndPw		Main charger power ground	Gnd	Gnd
M19	VbatCharger		Charger feature input supply	N.A.	N.A.
C16	CharInd		Charging indication(2)	Gnd	Gnd
K19	MainChSense		Main charger sense resistor (coil connection)	Gnd	Gnd
L19	MainChOut		Main charger sense resistor (battery connection)	Gnd	Gnd
	USB charger				
A13 B13 C13	Vbus		USB cable	N.A.	N.A.
A14 A15 B14	UsbCoil		USB external coil connection balls	N.A.	N.A.
B15 C14 C15	UsbGndPw		USB charger power ground	N.A.	N.A.

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
C19	UsbSense		USB sense resistor (coil connection)	N.A.	N.A.
B18	UsbOut		USB sense resistor (battery connection)	N.A.	N.A.
A16	VbusBis		Vusb LDO supply	N.A.	N.A.
	Coulomb counter				
U13	VinGauge			N.A.	N.A.
U12	GaugeSenseP		Gauge sense positive input	Gnd	Gnd
T13	GaugeSenseN		Gauge sense negative input	Gnd	Gnd
AB8500 multimedia features					
	Audio[3]				
F1	VinVaudio		Vaudio input power supply	N.A.	N.A.
G1	Vaudio		Vaudio LDO output dedicated to internal analog audio	N.A.	N.A.
F3	VddAudioTx		Audio transmit paths positive supply	N.A.	N.A.
E2	GndAudioTx		Audio transmit paths ground	Gnd	Gnd
T3	VddDigAud		Digital positive supply (1.2 V nominal) connected at pcb level at Vio12 output	N.A.	N.A.
U3	GndDigAud		Audio digital ground (Thermal Ball)	Gnd	Gnd
L1	VddAD_DA		Positive supply for all analog blocks except output drivers, must be connected to Vaudio ball	N.A.	N.A.
K2	GndAD_DA		Ground for all analog blocks except output drivers	Gnd	Gnd
M1	VddEar		Positive Supply for Earphone, EAR class AB output driver. It must be externally connected to Vaudio supply voltage ball.	VddAD_DA	VddAD_DA
M5	GndEar		Ground for Earphone, EAR class AB output driver	Gnd	Gnd
M9	GndMic		Ground for analog microphone amplifier	Gnd	Gnd
N1	VddHs		Positive supply for stereo headSet (HS) class AB output driver. It must be externally connected to Vaudio supply voltage ball	VddAD_DA	VddAD_DA

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
L2	GndHs		Ground for stereo headset class AB output drivers. This ball is used as headset voltage reference.	Gnd	Gnd
P1	VinVcphs		Positive supply for charge pump circuit. It can be connected directly to the battery.	Vbat	Vbat
R3	SmpsVcphs		Positive supply for charge pump circuit. It can be connected to Vsmps2.	Vio18	Vio18
N3	Cfhsp		Charge pump external capacitor positive pin	N.C.	N.C.
P3	Cfhsn		Charge pump external capacitor negative pin. Negative voltage tolerant ball.	N.C.	N.C.
P2	GndVcphs		Ground for charge pump circuit.	Gnd	Gnd
M6	VssVcphs		Negative supply output for headset drivers.	N.C.	N.C.
G3	VinVDmic		Vdmic input supply	Vbat	Vbat
M3	VssHs		Negative supply for stereo headset class AB output drivers. It must be externally connected to VssVcphs negative supply ball	Gnd	Gnd
G2	VAmic1		Low noise reference output voltage for analog microphone biasing	N.C.	N.C.
K1	VAmic2		Low noise reference output voltage for analog microphone biasing	N.C.	N.C.
F2	VDmic		Supply voltage output for up to 6 digital microphones	N.C.	N.C.
Y7	VinDclassInt		Supply for class D amplifiers. Can be connected directly to the most positive supply. (Battery) Note: VinDclassInt, VinVhfl, VinVhfr must be connected to the same supply voltage.	Vbat	Vbat
Y8	VinVhfR		Positive supply for Handsfree HFR class D output driver. Can be connected directly to the battery	Vbat	Vbat
Y6	VinVhfL		Positive supply for Handsfree HFL class D output driver. Can be connected directly to the battery	Vbat	Vbat

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
Y4	VinVibraInt		Supply for class D amplifiers. Can be connected directly to the most positive supply. (Battery) Note: VinVibraInt, VinVib1, VinVib2 must be connected to the same supply voltage.	Vbat	Vbat
AA2	VinVib1		Positive supply for VIB1 class D output driver. Can be connected directly to the battery	Vbat	Vbat
W4	VinVib2		Positive supply for VIB2 class D output driver. Can be connected directly to the battery	Vbat	Vbat
U8	GndVhfR		Ground for Handsfree HFR class D output driver	Gnd	Gnd
W7	GndVhfL		Ground for Handsfree HFL class D output driver	Gnd	Gnd
W3	GndVib1		Ground for VIB1 class D output driver	Gnd	Gnd
Y5	GndVib2		Ground for VIB2 class D output driver	Gnd	Gnd
J5 H5 J3 H3	LinLp LinLn LinRp LinRn		Stereo differential line input balls	N.C.	N.C.
H1 J1	Mic1ap Mic1an		Mono differential microphone input balls	N.C.	N.C.
J2 H2	Mic1bp Mic1bn		Mono differential microphone input balls	N.C.	N.C.
L3 K3	Mic2p Mic2n		Mono differential microphone input balls	N.C.	N.C.
J6	Dmic12Clk/ GPIO27	DO 50 K PD	Master clock output for digital microphones 1 and 2 or GPIO27	N.C.	N.C.
K6	Dmic12Dat/ GPIO28	DI 50 K PD	Multiplexed stereo input for digital microphones 1 and 2 or GPIO28	Gnd	N.C.
G6	Dmic34Clk/ GPIO29	DO 50 K PD	Master clock output for digital microphones 3 and 4 or GPIO29	N.C.	N.C.
H6	Dmic34Dat/ GPIO30	DI 50 K PD	Multiplexed stereo input for digital microphones 3 and 4 or GPIO30	Gnd	N.C.
F5	Dmic56Clk/ GPIO31	DO 50 K PD	Master clock output for digital microphones 5 and 6 or GPIO31	N.C.	N.C.

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
G5	Dmic56Dat/ GPIO32	DI 50 K PD	Multiplexed stereo input for digital microphones 5 and 6 or GPIO32	Gnd	N.C.
AA7 AA6 W9 AA8	HfLp HfLn HfRp HfRn		Differential stereo Class D outputs for Handsfree Speakers	N.C.	N.C.
L5 K5	Earp Earn		Differential mono Class AB output for earphone speaker	N.C.	N.C.
M2 N2	HsL HsR		Single-ended stereo ground-centered Class AB outputs for headset speakers	N.C.	N.C.
AA4 AA3	Vib1p Vib1n		Differential mono Class D output for Melody/Vibra1 functions	N.C.	N.C.
W5 AA5	Vib2p Vib2n		Differential mono Class D output for Melody/Vibra2 functions	N.C.	N.C.
T6 R6 P6 N6	Fsync0 BitClk0 DA_Data0 AD_Data0/ IntAudn	DI	Audio data Interface 0 (Note: AD_Data ball configured as interrupt, IntAudn, when internal audio FIFO used)	N.A.	N.A.
P5 R5 U5 T5	AD_Data1/ GPIO17 DA_Data1/ GPIO18 Fsync1/GPIO19 BitClk1/GPIO20	DI	Audio data Interface 1 or GPIO17 to GPIO20	Gnd	To Gnd through a 100k
	USB OTG transceiver				
E13	Vusb		Vusb LDO output dedicated to internal USB physical layer	N.A.	N.A.
F16	VddPHY		USB PHY supply	N.A.	N.A.
E14	VddUsbDig		Digital positive supply (1.2 V nominal) connected to VintCore12 ball	N.A.	N.A.
J13	GndUsbDig		USB digital ground	N.A.	N.A.
J19	VddUlpiVio18		ULPI IOs digital supply	N.A.	N.A.
E17	GndUlpiVio18		ULPI interface ground	N.A.	N.A.
C18	GndVbus		Analog USB interface ground	N.A.	N.A.
A20	DP		USB positive data	N.A.	N.A.
A19	DM		USB negative data	N.A.	N.A.
B19	ID		USB ID	N.C.	N.C.

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
D19	UlpiClk	DO	ULPI Clock	N.A.	N.A.
F19	UlpiDir	DO	ULPI direction	N.A.	N.A.
E19	UlpiStp	DI 100K PU	ULPI stop	N.A.	N.A.
B21	UlpiNxt	DO	ULPI next	N.A.	N.A.
B20 C21 C20 D20 D21 E20 E21 F20	UlpiData[7] UlpiData[6] UlpiData[5] UlpiData[4] UlpiData[3] UlpiData[2] UlpiData[1] UlpiData[0]	DI 50K PD	ULPI data	N.A.	N.A.
	General purpose ADC, Accessory detection				
R20	VddADC		General purpose ADC supply	Gnd	Gnd
N13	GndADC		Internal ADC ground	Gnd	Gnd
N16	BatTemp		Battery temperature	To Gnd through a 47k	To Gnd through a 47k
T12	AdcAux1		ADC Auxiliary input	Gnd	Gnd
T11	AdcAux2		ADC Auxiliary input	Gnd	Gnd
P16	AccDetect1		ADC and Accessory detection 1 input	N.C.	N.C.
P17	AccDetect2		ADC and Accessory detection 2 input	N.C.	N.C.
N5	GPADCTrig	DI 50K PD	ADC trigger input	Gnd	Gnd
	TVout interface				
L17	VinVTVout		**VTVout** input power supply	Vbat	Vbat
M17	VTVout		VTVout ldo output dedicated to internal TVout.	Gnd	N.C.
V21	VPLLIn		TVout PLL supply	Gnd	Gnd
R21	VddDAC		CVBS DAC supply	Gnd	Gnd
L10	GndDAC		CVBS DAC ground	Gnd	Gnd
K17	VddDigDenc		Digital Positive supply (1.2 V nominal) connected at pcb level at Vio12 output	Gnd	Gnd
L13	GndDenc		DENC digital ground	Gnd	Gnd
W20	CVBS		Video Composite signal output	Gnd	Gnd

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
AA19 W18 AA20 Y18	YCbCr3/ GPIO9 YCbCr2 / GPIO8 YCbCr1 / GPIO7 YCbCr0 / GPIO6	DI	Time multiplexed 4:2:2 luminance and chrominance data with synchro embedded (Dual data rate data transfer)	Gnd	To Gnd through a 100k
	SIM interface				
B12	VinVsim		Vsim input power supply	N.A.	N.A.
A12	VbatVsim		Vsim input power supply	N.A.	N.A.
C12	Vsim		Vsim LDO output dedicated to SIMcard supply	N.A.	N.A.
F10	CUiccDetect		SIM card detection (active low)	N.A.	N.A.
E10	CIsoReset	DO WeakPD	SIM card reset ball	N.A.	N.A.
F11	CIsoClock	DO WeakPD	SIM card clock ball	N.A.	N.A.
E12	CIsoData	DO WeakPD	SIM card data	N.A.	N.A.
F12	CUsbDp	DI 90K PD	SIM card DP ball	Gnd	N.C.
E11	CUsbDm	DI 90K PD	SIM card DN ball	Gnd	N.C.
AA18	UsbUiccPd / GPIO11	DI	UsbUicc Pull down control or GPIO11	Gnd	N.C.
G16	IsoUiccIOCtrl	DI 50K PD	ISO-UICC IO direction control	N.A.	N.A.
F17	IsoUiccClk	DI 50K PD	ISO-UICC clock	N.A.	N.A.
H16	IsoUiccData	DI 50K PD	ISO-UICC data	N.A.	N.A.
G17	IsoUiccInt	DO Low Level	ISO-UICC output interrupt or reset	N.A.	N.A.
H19	UsbUiccDir/ Gpio21	DI	USB-UICC IO direction control / Gpio21	Gnd	To Gnd through a 100k
G20	UsbUiccData/ Gpio22	DI	USB-UICC data or DP / Gpio22	Gnd	To Gnd through a 100k
G19	UsbUiccSe0/ Gpio23	DI	USB-UICC SE0 or DN / Gpio23	Smps2 (1.8 V)	Smps2 (1.8 V)

Table 20. Ball connection if feature is unused (continued)

Ball #	Name	State after reset	Comments	Unused feature	
				Phone in production	During phone development
Miscellaneous and test					
	Miscellaneous				
U16	GPIO12	DI	GPIO12	Gnd	N.C.
W17	GPIO13	DI	GPIO13	Gnd	N.C.
M16	GPIO26	DI 50K PD	General purpose IO	Gnd	N.C.
R17	GPIO34	DI 50K PD	GPIO34	Gnd	N.C.
W15	GPIO35	DI 50K PD	GPIO35	Gnd	N.C.
F15 B17 F14	PWMOut3/ GPIO[16] PWMOut2/ GPIO[15] PWMOut1/ GPIO[14]	DO	PWM outputs / GPIOs	N.C.	To Gnd through a 100k
	Test				
T17	Test1		Must be connected to ground	Gnd	Gnd
F8	Test2		Must be connected to ground	Gnd	Gnd
U11	HVFuse		Must be left opened i	N.C.	N.C.

1. Interrupts not masked
2. Warning: ILED current source will be ON when charger is in hardware mode, Battery voltage below VbattOk2R threshold. In Sw mode, to avoid to draw ILED to ground, it is recommended to disable LED indicator.
3. In this table it is considered that at least one audio feature is used.

6 Revision history

Table 21. Document revision history

Date	Revision	Changes
14-Nov 2011	1	Initial release